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MODELING ELECTROMAGNETIC EFFECTS IN MMICs FOR T/R MODULES

CALSPAN-UB Research Center

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Griffiss Air Force Base, New York

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13. ABSTRACT (Maximum 200 words)
This report documents an investigation of circuit modeling of electromagnetic environment effects (E3) in the microwave monolithic integrated circuits (MMICs) contained in T/R models. The work was performed at Rome Laboratory under an Expert Science and Engineering contract with Calspan/University of Buffalo Research Center. Topics include multi-port vector characterizations, data acquisition, CAD testing and validations of models for selected MMICs (and models), and recommendations and plans for further assessments of E3 in advanced MMICs, T/R modules and multi-chip (MCM) modules. An extensive bibliography on contemporary MMIC design and GaAsFET modeling is also included.

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DANIEL J. KENNEALLY
January 26, 1993

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INTRODUCTION

An Expert Science and Engineering (ESE) contract was initiated by the Rome Laboratory at Griffiss AFB, NY with the Calspan/U. of Buffalo Research Center in January 13, 1992. Its purpose was to perform investigations of CAD modeling of Electromagnetic Environmental Effects (E3) in microwave monolithic integrated circuits (MMICs) and in related transmit and receive (T/R) modules. The objectives of the effort were:

1) to investigate vector susceptibility concepts for use in modeling E3 in multi-port MMICs;

2) to provide modeling assistance to the Rome Laboratory, as needed;

3) to validate the vector circuit susceptibility concepts using MMIC data selected from current T/R modules; and,

4) to provide a road map, or design plans for further E3 analyses and assessments of T/R modules and their ICs.

This effort was completed on January 9, 1993. This final report for the effort is now submitted in accordance with the contract requirements.

This report is organized as follows. A background to the problem is first given which places this modeling effort into some proper (and admittedly, somewhat subjective) perspectives of Air Force system applications. These necessarily focus on transmit/receive (T/R) modules used in advanced, phased array antennas. Next, a vector concept for characterization of the electromagnetic environmental effects in multi-port MMICs is introduced and developed. It is about the theoretical modeling of multi-ports and provides analytic context for validation. A hypothetical system level model is also presented and used as a performance benchmark.

The main body of results are contained and described in the tasks 1-4 sections together with their appendices A and B which contain related and other supporting data. A lengthy section containing an extensive bibliography on CAD analyses and modeling of contemporary MMICs and T/R modules is presented. This is an up-to-date compendium of open literature which is currently available on MMIC circuit modeling and related topics. It contains many useful references to circuit E3. This bibliography by itself should be an especially useful adjunct to the design literature.

Finally, a summary and recommendations section contains brief, executive style descriptions of the most significant work accomplished and appropriate recommendations. These executive level, summaries and recommendations are organized by contract tasks for convenience of the readers.

BACKGROUND

Advanced systems such as MILSTAR, ASTAR, and SBR will use the new MMIC circuit technology in phased array antennas that will likely be platform conformal. These MMIC devices must be reliable and RF robust to survive in the electromagnetically dense and degrading, wideband RF environments.

This is especially true for the conformal, phased array antennas where the MMIC devices and modules will be physically close to each other, to other emitters on the platform, and to the electromagnetic environment itself.

T/R modules are the vital building blocks of the active aperture, phased array antennas used for advanced communications and radar systems. They operate in environments where unintended electromagnetic environmental spectra cause signal upset, distortion, degraded noise performance, antenna pattern control errors and other types of upset or damage in victim circuits and modules.

Modeling and measuring E3 susceptibility of T/R modules and MMICs to electromagnetic environmental effects (E3) are important technology initiatives in the Electromagnetic Systems Division (ERP) of the Rome Laboratory.

For example, a vector characterization to account for the E3 susceptibilities at all ports of the victim MMICs and modules which include DC bias, RF signal, grounds, digital control ports, and any on-board BIT ports that typically make up a T/R module. Modeling should account for E3 induced, vector distortion susceptibility at any MMIC or module ports.

"E3 vector distortion" in a multi-port, MMIC device is defined here as the response at any admissible port in which a deviation from the device's baseline, specified performance is caused by any E3 power source that is "wire" connected or "field" connected to any other port on the same device.

"Baseline performance" of a MMIC device is defined as the set of measured or specified parameters that describe the device's normal operation within some "designed-to" performance envelope.

"Admissible ports" are any accessible ports (or pin pairs) on the MMIC package which permits entry of E3 energy when operating in its intended environment.

VECTOR CHARACTERIZATION OF E3 IN MULTI-PORT MMICs

MMIC device susceptibility to unwanted, interfering signals is usually determined using CAD tools by simulating (extraneous) test signals, adding them to the desired signals at the input signal port, and then computing the contaminated response at the output signal port.

This susceptibility characterization is interactively scalar. It involves only two signal ports on the MMIC device - the RF input and output ports. The problem with this is that most MMIC chips are multi-port, packaged devices with a mix of RF, IF, digital, ground, bipolar DC bias, and other type ports.

A nonlinear vector susceptibility model of a MMIC must be able to simulate the mixing and cross coupling of desired signals present at the input port with any undesirable signals that may also be present at the input port or at any other port or combination of ports.

The MMIC response is then the nonlinear distortion at the output signal port and at any other port or combination of ports. A susceptibility matrix thus should include all the accessible ports (or pin pairs) of a packaged MMIC.

Conventional assessments of electromagnetic environmental effects (E3) in active networks typically use Intermodulation Distortion (IMOD) and Cross Modulation Distortion (XMOD) tests in the lab that can characterize and measure the onset of the nonlinear, degraded performance.

For microwave monolithic integrated circuit (MMIC), it is common practice to combine extraneous E3 signal spectra with the desired signals at the input port. This produces a corrupted signal response at the output port and it is a useful measure of the degraded circuit performance of the victim device due to the E3 spectra.

This traditional way of characterizing E3 in active devices is basically scalar. It is nominally used for testing assessments of IMOD and XMOD in two-port networks only. MMIC chips and modules in contrast are multi-port RF devices with digital, ground, and bipolar DC ports, as well. The digitally controlled phase shifter, T/R switches, and mixers as well as the low noise, linear preamps and power amplifiers are just some of the more representative MMIC multi-ports used in T/R modules.

The initiative for this work was the need for modeling formalisms of E3 in multi-ports. Previous analyses and tests on low noise, MMIC preamplifiers from prototype T/R modules were done at Rome Lab using a LIBRA software circuit simulator [1]. The results indicated that extraneous E3 spectra injected at any arbitrary MMIC port, intended or otherwise, can couple to and corrupt the desired signals at the output port.

Cross coupling extraneous E3 spectra from any MMIC port to any other port which then causes IMOD, XMOD, etc. at the other ports (via intrachip nonlinear transfer paths), in addition to the signal input-output port pair, suggested that a matrix description might characterize E3 induced, multi-port effects. Thus, the concept of a "vector" characterization of a multi-port for E3 assessments and analyses was conceived and formulated.

Low noise preamplifiers, power amplifiers, microprocessor controlled phase shifters, and PIN diode switches are among the other T/R module subfunctions of interest. A vector modeling base should probably start with individual chip functions and attempt to build up a library of vector models for each one. Then, groupings or chip sets for various chip functions could be investigated with the intent to eventually integrate them into a composite model of a T/R module.

The vector models' magnitude and phase responses at the output signal port(s), or at other response ports of interest, due to CW multitone E3 driver(s) coupled into any arbitrary port (or ports) should also be investigated. A vector E3 model of the multi-port should predict the resulting signal distortion at the output signal port. Also, degrading circuit (performance) effects, including DC offsets, at any other port(s) due to arbitrary E3 spectral drivers should also be considered.

While these descriptions of the modeling problem and possible approaches may be implied as frequency domain, and thus consistent with common measurements practices, they should not be constrained to the frequency domain. A time domain methodology for E3 assessments of microwave multi-ports is a viable alternative. In fact, the extensive work done previously on power series modeling represents considerable good evidence of this validity of a time domain approach.

Moreover, any time domain approaches to MMIC modeling would still have to be reconciled to contemporary CAD practice in industry, especially in those areas of tests and specifications of device performance where most of the data are still frequency domain.

The Electromagnetics & Reliability Directorate (ER) of the Rome Laboratory is committed to improving the electromagnetic compatibility and related reliability of the MMICs and digital ICs used in radar T/R modules. These initiatives include multi-chip modules (MCMs).

Some of the MMIC programs actively supported at present include DoD and DARPA CAD/CAM initiatives and other related Rome Lab contracts, as well as some vigorous internal lab efforts in reliability and compatibility. The latter generally focus on the computer-aided analyses and measurements of both baseline and E3 performances of the circuit chip suites used in Rome Lab's T/R modules and MCMs.

These include thermal, electromagnetic, packaging, interconnects, failure physics, test diagnostics, and other efforts in MMICs, digital ICs, and the other circuit components contained in a typical T/R module. Electromagnetic Environmental Effects data and other related thus obtained are used for E3 and electromagnetic compatibility performance assessments of individual MMIC chips and the composite T/R module.

The intent is to develop the technical bases and supporting data for future follow-on contractual efforts (and for related in-house initiatives) to provide E3 mitigation design techniques at the device and module levels. In addition, these efforts also serve the needs for aggressive programs of technology transfer to commercial users as required.

SUSCEPTIBLE SYSTEM MODEL

To illustrate the problem at system level, a hypothetical (system) victim was postulated. The assumed system model is based upon the following transmit and receive parameters for a victim radar designed and implemented with advanced circuit T/R modules:

X-Band Radar	9-10 GHz
Pulse Width	3 us
Duty Cycle	.01 %
Receive Power Density at Module Antenna	30.0 dBm/sq cm
RCS of Module Antenna	2 sq cm
T/R Module Losses (antenna to GaAsFET)	13.5 dB
Circuit safety Margin	10 dB
Peak Threshold Level	43 dBm
Average Threshold Level	3 dBm

Then, an approximate computation using the above data and available measurements data [2] suggest that a victim GaAsFET in a T/R module of our radar system can expect some damage and/or upset. It may occur for incident threshold levels of about 43 dBm peak power at the susceptible FET device pins. This threshold level corresponds to 3 dBm of average power.

Compared with power levels reported in the literature where some comparable susceptibilities range in power levels from +20 dBm to -20 dBm of average power, the above estimated levels do not seem to be too far out of line. They then are the initial guidelines for this study.

A problem with making these kind of assessments is the conflict between choosing "top-down" or "bottom-up" competing approaches. For example, we are ultimately interested in the total E3 power or energy levels that are eventually present at the MMIC ports. These undesirable E3 spectra can come from several sources internal or external to the modules, or both. The E3 sources may be wire conducted or field connected to the victim ports.

Beyond this particular T/R module is a whole array of other identical modules that are phased together, and otherwise interconnected with extensive platform cabling for RF, power, and digital control. And, that antenna array may be conformal on a very flexible and mechanically dynamic platform, rich with other electromagnetic emitters.

The platform itself may be immersed in an intense electromagnetic environment also rich with emitters, some friendly and some not. This total environment exterior to the platform is just part of a complex chain of many interacting E3 sources.

Thus, these E3 signal spectra in this hypothetical bottoms-up, system flow, basically encounter what may be viewed as path "transfer functions" on the way back "up" to their environmental sources. In this concept, E3 spectra at a victim port can be related to its immediate "environment" through linear spectral transformations which are familiar to most engineers.

The problem with these "top-down" and "bottom-up" approaches is that those system transfer functions are not known. We may measure or specify the platform exterior environment but without system transfer functions, the E3 spectral power levels ultimately arriving at the ports of a potentially susceptible MMIC are not known.

An extensiv measurement program might help alleviate the problem of unknown MMIC susceptibility levels, to some extent, provided that the suitable spectral data were taken throughout the suspected paths (assuming they were "known") anywhere on and in the given system platform when it is driven by given exterior environmental sources.

With "enough" spectral data taken at "enough" interior points, the transfer functions of these intervening coupling paths may be identified with enough accuracy to predict the offending E3 levels that ultimately reach the ports of a particular MMIC device. Thus, using these kinds of system data, E3 susceptibility analyses could be based on realistic power levels, rather than simply finding those input spectral levels at a MMIC that cause the upset and distortion.

TASK 1 - VECTOR MODELING OF MULTI-PORTS

Modeling, simulating and measuring the E3 susceptibility of T/R modules and their constituent MMICs and digital ICs, represent challenging technology initiatives. In our approach here, the circuit models we seek for vector characterizations of E3 in MMICs and T/R modules are more heuristical rather than explicitly analytical.

Heuristic circuit models are any mathematical abstractions, concepts and data that describe the device behavior at the circuit ports, rather than the exact algorithms that explicitly contain (and solve) the device state matrix equations. Heuristic models in this sense are more pragmatic, and are given some precedence over those explicit analytical models which contain exact solutions of the MMIC FET state equations. The latter are usually derived and solved from solid state physical models.

While analytical models may not be as yet be analytically "formulated" nor rigorously derived for multi-port MMICs, heuristic circuit models are justified with empirically based, intuitive reasoning. Of course, that rationale must be based on sound engineering evidence which may be empirical, historical or mathematical data that are "plausible" if not rigorously proven.

Mathematical abstractions, equations, concepts, or just simply descriptive CAD performance data are all allowed. These can shed useful insight and meaning to a model behavior at the circuit or module ports instead of using explicit algorithms to embody (and solve) the state equations at the ports involved. In this sense, they are performance macromodels at the ports of interest.

This task reviewed the classical power series models for memory-less (resistive) systems. A classical power series uses one-dimensional, algebraic polynomials as time domain, driving point functions for the one-ports; or alternatively, as time domain, transfer functions for the two-port networks.

Next, a power series for systems with memory, (i.e. capacitive and inductive), was investigated to provide the necessary time delay or frequency domain phase shift. It is a generalized power series with time delay terms which permits multi-port systems with memory.

The reasons for starting at a classical approach and working up to the more generalized series are as follows. First, it offers a plausible, easy way to extend a memory-less model to networks with memory. Second, it provides a good intuitive understanding of the cross mixing (i.e., the signal intermodulation and cross modulation) processes that occur in the coupled ports of multi-port MMIC. Lastly, it provides a more familiar starting point to more advanced, multi-port Volterra modeling which uses familiar scattering parameter concepts and related spectral analyses. This transition to Volterra is also very well documented.

In a Volterra modeling approach the sequence would be to first use a discrete version for a one-port with its polynomial coefficients as complex constants, proceed to a generalized multi-port and then to proceed to the continuous, distributed Volterra model that uses familiar power dependent, scattering parameters [3]. This might clarify very theoretically demanding mazes that easily tend to obscure the effects of interest.

The classical power series model for resistive n-port MMIC systems contains n-dimensional, time domain polynomials of a degree n*1, where n is the number of MMIC ports involved and 1 is the highest degree of the nonlinearity in the driving ports or in the cross coupled ports. We assume that the degree of the port nonlinearities is the same for all of the total N ports on the MMIC.

The generalized power series for other systems with memory (i.e. capacitive and inductive) [4] was also considered but seemed to be too unwieldy for our purposes. This power series, however, does provide the needed time delay and phase shift for possible time and frequency domain models, respectively.

E3 Characterizations

In a vector modeling approach, a linear characterization or a baseline model of the MMIC is first formulated and computed. It uses familiar linear n-port, S-parameters where Sjj is the complex input reflection coefficient at port jj and Sij is the complex transfer coefficient between ports j and i. The latter may have a negative magnitude for the transmittance of an active amplifier. The indices run from i=j=1 to i=j=n where n is the number of MMIC port of interest.

The baseline models are then run on the CAD circuit simulator of choice and the resulting linear performance compared with available measured data. When there are differences of note, it is usually the linear model parameters that are selected for corrective tweaking.

Next, a quadratic nonlinear characterization or model is computed and/or measured using both the linear S-parameters and the measured or computed power transfers (i.e., from second order, nonlinear transfer functions) at the second order mix frequencies for all the input frequencies at all the MMIC ports of interest. The highest degree of a quadratic nonlinearity is by definition l=2.

The above should then give the mix powers generated by the l=2 nonlinearities at any response port, given: the signal spectra at the input port, the linear and nonlinear transfer functions among all the ports; and, the E3 spectra at the extraneously driven port(s).

These mix powers should also contain intermodulation and cross modulation terms for the power coupled from the extraneous ports to the desired signal ports. This is the concept of a quadratic vector characterization.

This conceptual process or heuristic algorithm can be extended to include the cubic, quintic, quartic,...,"Lth-ic" responses, i.e., all the higher order, nonlinear characterizations for l=0 (DC) to l=L, the highest degree of nonlinearity in the MMIC. It is a numerical process that bootstraps on the results from the previous lower order or degree terms in a set of nonlinear, transfer function polynomials. The end result should be a vector set of linear and nonlinear, transfer functions for finding (at least, in principle) the mix powers outputted at any MMIC response port, for any spectral power inputted at any signal input port or at any combination of ports.

This then is the concept of the generalized vector characterization for a multi-port MMIC with an Lth degree of nonlinearity in each of n-ports. We now develop this theme in some detail.

For example, it is quite common in a bilateral amplifier device to consider (or to assume) the transfer function between its input and output signal ports to be linear. "Linear" suggests a transformation in which the output spectral vectors differ from the input spectral vectors only in magnitude and phase; i.e., the frequency vector is preserved in a linear transformation.

One common test for these nonlinearities (or onset of nonlinear behavior in an otherwise assumed linear network) is to add an off-tune signal to the desired signal at the input port and then to measure or compute the resultant distortion response at the nominal output port. This gives the familiar scalar intermodulation and it involves circuit nonlinearities that make up the amplifier's forward transfer function.

Another test adds the extraneous signal, either in-band or out-of-band, to some other unintended port of the amplifier such as the bias or ground rail ports, and measures or computes a resulting distortion response at the desired signal output port.

This now involves a "cross modulation on the desired signal from an unwanted E3 source that is not directly connected to the input signal port. These two ports are really "connected" by the nonlinear, cross coupled transfer function of the amplifier now acting as a three-port mixer.

The vector modeling task used the classical power series approach for memory-less circuits. Many of these models were developed elsewhere; see for example [5]-[7]. These models describe the response of a nonlinear, resistive network using a polynomial characteristic to relate an independent input variable, such as a port voltage, with a dependent response variable such as current at the same driven port or at some other port.

This means that with both the dependent and independent variables defined at the same port, we have essentially a one-port, driving point resistance model. With one variable defined at one port and the other variable defined at some other port (as in figure 2), we would have a two-port transfer characteristic or a "transresistance" for a resistive, two-port model. And by polynomial inversion, independent and dependent variables can be reversed to admit the voltage nonlinearities for one and two-port conductance models.

Figure 1 illustrates a black box model for a resistive, one-port device with an l-th degree power series for a current nonlinearity and which is truncated at l=L.

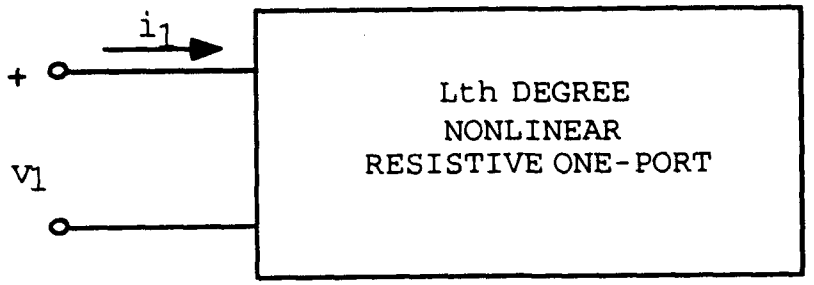


FIGURE 1

where

$$v_1 = \sum_{j=0}^{L} a_j [i_1(t)]^j \qquad (1a)$$

or

$$v_1 = a_0 + a_1 i_1(t) + a_2 i_1^2(t) + a_3 i_1^3(t) + \ldots a_L i_1^L(t) \qquad (1b)$$

For a single input, sinusoidal current tone in equation (1), even degree terms of its nonlinearity give rise to both DC offsets and even harmonics in the voltage responses. The odd degree terms give rise to the odd harmonics in the voltage response. This is probably the simplest and most common of nonlinear, classical models.

Extending this classical model to a resistive n-port network is straight forward. It involves developing a mathematically consistent set of n simultaneous, n-dimensional polynomials each of degree N*L, where N is the total number of MMIC ports and L is the highest degree of MMIC port nonlinearities. For simplicity, the highest degrees of nonlinearity are assumed to be the same for all the n = N ports.

The total modeling set contains a total of N polynomial equations for Jacobian completeness. The case for N=2 and L=3 for a cubic 2-port was worked out in detail. It is clear that the resulting spectral content of all the possible mixes and its attendant complexity grows very rapidly with n and l.

To illustrate this point, we will consider this cubic in some detail. Figure 2 illustrates a model of a generalized, 2-port (N=2) with the Lth degree nonlinearity of each port the same degree l=L.

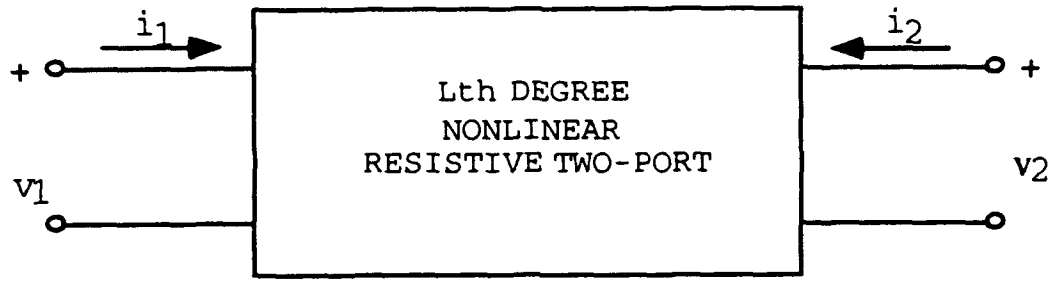


FIGURE 2

where

$$v_1 = \sum_{j=0}^{L} \sum_{k=0}^{L} a_{jk}[i_1(t)]^j[i_2(t)]^k$$

and

$$v_2 = \sum_{j=0}^{L} \sum_{k=0}^{L} b_{jk}[i_1(t)]^j[i_2(t)]^k \qquad (2)$$

Then with equation (2) for the cubic nonlinearity of degree L=3 taken at each one of the two ports, we would have:

$$\begin{aligned} v_1 = {} & a_{00} + a_{01} i_2 + a_{02} i_2^2 + a_{03} i_2^3 + \\ & a_{10} i_1 + a_{11} i_1 i_2 + a_{12} i_1 i_2^2 + a_{13} i_1 i_2^3 + \\ & a_{20} i_1^2 + a_{21} i_1^2 i_2 + a_{22} i_1^2 i_2^2 + a_{23} i_1^2 i_2^3 + \\ & a_{30} i_1^3 + a_{31} i_1^3 i_2 + a_{32} i_1^3 i_2^2 + a_{33} i_1^3 i_2^3 \end{aligned}$$

and

$$\begin{aligned} v_2 = {} & b_{00} + b_{01} i_2 + b_{02} i_2^2 + b_{03} i_2^3 + \\ & b_{10} i_1 + b_{11} i_1 i_2 + b_{12} i_1 i_2^2 + b_{13} i_1 i_2^3 + \\ & b_{20} i_1^2 + b_{21} i_1^2 i_2 + b_{22} i_1^2 i_2^2 + b_{23} i_1^2 i_2^3 + \\ & b_{30} i_1^3 + b_{31} i_1^3 i_2 + b_{32} i_1^3 i_2^2 + b_{33} i_1^3 i_2^3 \end{aligned} \qquad (3)$$

Note that in equation (3) for the cubic:

(a) the highest degree of cross modulation occurs between i1 and i2 in the terms with a total degree equal to the sum of each variable: in this case, the total degree is equal to 6 (degree 3 from i1 and degree 3 from i2).

(b) the two port interaction requires a two-fold summation of products involving i1 and i2. In general, an n-port will require an n-fold summation.

(c) the total number of terms equals (L+1)(L+1), so that for a cubic nonlinearity we have a total of 16 terms from each of the two port polynomials to add.

(d) the sum of j+k indices gives the degree of the term with the coefficients of ajk or bjk in the cubic two-port.

(e) coefficients with the indices k=0 denote terms of the harmonic driving point resistances, relating v1 to i1 at the same port.

(f) coefficients with the indices j=0 denote terms of the harmonic transfer resistances (or the "transresistances") relating v1 at port one to i2 at port two.

(g) coefficients with the nonzero indices of any j and any k denote the cross modulation resistances, relating v1 to the power mixes of i1 and i2 at ports one and two, respectively.

(h) a cubic two port will, in general, contain at least two polynomial equations with a total of 32 terms as follows:

2 DC terms:

$$a_{00}, b_{00}$$

4 linear terms:

$$a_{10}i_1, a_{01}i_2, b_{10}i_1, b_{01}i_2$$

6 quadratic terms:

$$a_{20}i_1^2, a_{11}i_1i_2, a_{02}i_2^2,$$
$$b_{20}i_2^2, b_{11}i_1i_2, b_{02}i_2^2$$

8 cubic terms:

$$a_{30}i_1^3, a_{21}i_1^2 i_2, a_{12}i_1 i_2^2, a_{03}i_2^3,$$
$$b_{30}i_1^3, b_{21}i_1^2 i_2, b_{12}i_1 i_2^2, b_{03}i_2^3$$

6 quartic terms:

$$a_{31}i_1^3 i_2, a_{22}i_1^2 i_2^2, a_{13}i_1 i_2^3,$$
$$b_{31}i_1^3 i_2, b_{22}i_1^2 i_2^2, b_{13}i_1 i_2^3$$

4 quintic terms:

$$a_{32}i_1^3 i_2, a_{23}i_1^2 i_2^3,$$
$$b_{32}i_1^3 i_2, b_{23}i_1^2 i_2^3$$

2 sextic terms:

$$a_{33}i_1^3 i_2^3, b_{33}i_1^3 i_2^3$$

Figure 3 illustrates a generalized resistive n-port with an L-th degree nonlinearity at each of N ports.

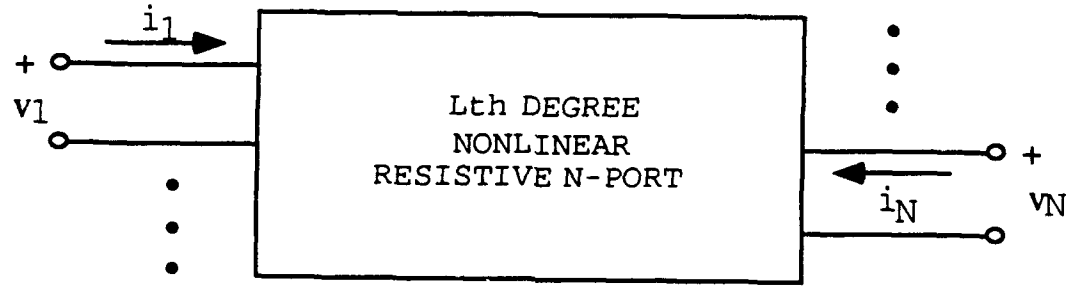


FIGURE 3

where

$$\left.\begin{aligned} v_1 &= \sum_{j=0}^{L} \cdots \sum_{l=0}^{L} a_{j\ldots l}[i_1(t)]^j \ldots [i_N(t)]^l \\ &\vdots \\ v_N &= \sum_{j=0}^{L} \cdots \sum_{l=0}^{L} \gamma_{j\ldots l}[i_1(t)]^j \ldots [i_N(t)]^l \end{aligned}\right\} \quad (4)$$

Note that:

(a) equation (4) contains N polynomials for N independent variables in the N dependent variables (v1, v2, v3,.....vN).

(b) the highest degree of cross modulation occurs in those terms with degree equal to N*L where N is the number of ports and L the highest degree of nonlinearity in each MMIC port.

(c) the presence of n=N ports requires an N-fold summation of products of the independent variables i1, i2, i3,....iN.

(d) the indices with j=0 are harmonic transfer coefficients.

(e) the indices with k=0 are harmonic driving point coefficients.

(f) indices with any nonzero j and k are cross modulation coefficients relating port j to port k modulation transfers.

Extending this classical approach involves finding a power series for (reactive) networks with memory, i.e. those with capacitance and inductance which is more likely the case. There is such a series in the literature. It is a generalized power series [4] with delay terms in its transfer polynomials.

Converting the above models to ones with memory would require that the time variables in t be replaced with a time shifted variable (t-T) in equations 1-4, where T is now some constant time delay associated with each memory port. In a more general case, T could be different for each port as they are the (time) equivalent of the phase shifts in the frequency domain.

In the more generalized power series approach, one-ports with memory are readily modeled. It should be applicable to multi-ports. Thus, this approach takes the classical approach for systems and circuits with no memory and applies it to those with memory. It seems apparent that the classical series approach is just a special case of this more generalized power series approach.

The approach is to develop a heuristic MMIC model(s) using the generalized power series approach and to relate them to discrete (or constant coefficient) element and distributed (or functional coefficient) element versions of the generalized Volterra Series models. For example, summations of discrete elements should go over as continuous integrations for distributed elements in the Volterra case.

Rome Laboratory as RADC pioneered the Volterra approach in the 70's to model nonlinear communications two-ports. While successful, the Volterra approach required a very large number of terms to converge in some finite time on finite machines.

The approach of classical power series to more generalized power and Volterra series is pragmatic. It provides a plausible extension of the memory-less model and provides good, intuitive understanding of cross mixing processes among the coupled MMIC ports. It is a likely starting point for Volterra modeling using modified scattering parameters familiar to microwave engineers.

The Volterra series approach and harmonic balance methods involve some demanding theoretical mazes which may obscure the circuit (E3) effects of interest. Discrete versions of Volterra and power series are then smooth transitions to more generalized Volterra series and harmonic balance methods.

In spite of its convergence penalties, Volterra series does allow modified linear and nonlinear S-parameters to characterize E3 performance of MMICs. Considerable data [8] indicate that scattering parameters best describe circuit responses associated with E3 as unintended spectral changes from the intended, design-to-performance. Related effects can also induce shifts in FET bias points which then change the small signal S-parameters.

In summary, assessments of nonlinear effects can make use scattering parameter concepts familiar to most engineers. The ultimate goal is a Volterra modeling with harmonic balance in a (heuristic) model that does not tax ones' theoretical stamina. It should describe port behavior of any active, multi-port MMIC and be conceptually valid for larger, more complex T/R modules.

While the vector modeling for resistive, memory-less multi-ports was completed, the more generalized time domain matrix formulation could not be derived nor its corresponding solution vectors be found with the available resources of this effort. This is not surprising in view of the many (!) driving point and transfer function nonlinearities that must be accounted for when considering all the interactive ports of a multi-port MMIC.

The n-port, memory-less model provides good insight into the problem. Cross modulation occurs among all the MMIC ports connected with nonlinear transfer functions. This XMOD depends on the number of coupled ports and the highest degree of (like) nonlinearities involved in the cross coupling. Thus, it takes N polynomials of degree L to characterize all of the independent, time domain response variables in a multi-port MMIC.

Although the large polynomials necessarily involved suggest convergence problems, and some did occur in validation, a vector formulation of E3 in MMIC appears plausible and useful. The generalized power series approach is shown valid and exhibits good engineering utility for E3 assessments of multi-port MMICs.

Nonlinear spectral analyses were not attempted. While the theoretics may be elusive, the vector validation task did use commercial harmonic balance, spectral methods [1, 9] with good success. Those results are contained elsewhere in this report.

TASK 2 - MODELING ASSISTANCE

Rome Laboratory (ERP) was provided with a brief review and E3 critique of a common high density, interconnect process for MCM (multi-chip module). A brief summary follows. High density packaging interconnects bare IC chip dice into a module by a process of embedding, passivating, bonding and wiring them into multiple layers of ceramic substrates which are then tiered or stacked in succession to form the multi-chip module. Three E3 related issues were so identified:

1) Since both digital and linear ICs are included in MCM, mixed mode, E3 measurements are needed to obtain MCM module performance characterizations. This suggests hybrid measurements issues for characterizations of the E3 in MCMs.

2) Because of the high density of mixed mode, active components per tier and the inherent need for multi-tiered interconnects, vias and other bridges, the stray (parasitic) intracoupling in the module now becomes a three dimensional modeling issue. This may present a serious obstacle to MCM modeling because most contemporary circuit CAD is planar.

3) The increased complexity and density of the active components and their associated interconnect wiring also suggest new issues of coupling into and within a module that will further increase its latent susceptibility to E3.

At the request of Rome Lab (ERP), we attended a three day work shop on Integrated Test Diagnostics which was sponsored by and held at the Rome Laboratory. This provided a very helpful overview which helped to discover some interesting new aspects of E3 in multi-chip and T/R modules. A report on this activity is included as appendix A.

We visited Raytheon/Andover MA to review in-house design and foundry capabilities for MMICs and T/R modules. The exchange of data and design information on their current programs was very productive. We obtained circuit files on disk in TOUCHSTONE [9] and LIBRA formats for a power amplifier (PA) MMIC used in a typical T/R module. We also tried to obtain measured performance data that confirm or validate the MMIC circuit design and prediction models used by Raytheon CAD work.

There were few surprises in the way Raytheon does its CAD work. We already had a good preconception of most current industry practices from the open literature, and from other personal contacts. They use interesting nonlinear FET models.

Raytheon was quite open with design data up to a point: "Materka" GaAsFET models which have considerable design success were not given to our clients. These Raytheon models are proprietary sensitive. But we did gather enough information to make "some" intelligent guesses to allow our client to devise an "equivalent" nonlinear model of the PA GaAsFET.

Rome Lab indicated to us that the present contractual effort was very relevant to the electromagnetic effects' tracks planned (by the Rome Lab) for a local IEEE symposium scheduled in June of 1993. At Rome Lab request, we submitted three paper abstracts to that upcoming conference. They are; "Modeling E3 in MMICs", "Coupling Modes of E3 to MMICs", and "E3 Design Issues in MCMs and T/R Modules". Since these papers are representative of the current work, publishing the resulting data should be beneficial to all parties concerned.

TASK 3 - VECTOR MODELING VALIDATIONS

This task attempted to validate the vector models with appropriate E3 power simulated into selected MMICs from the T/R modules. Circuit parameter types and value ranges for characterizing the baseline MMICs were identified.

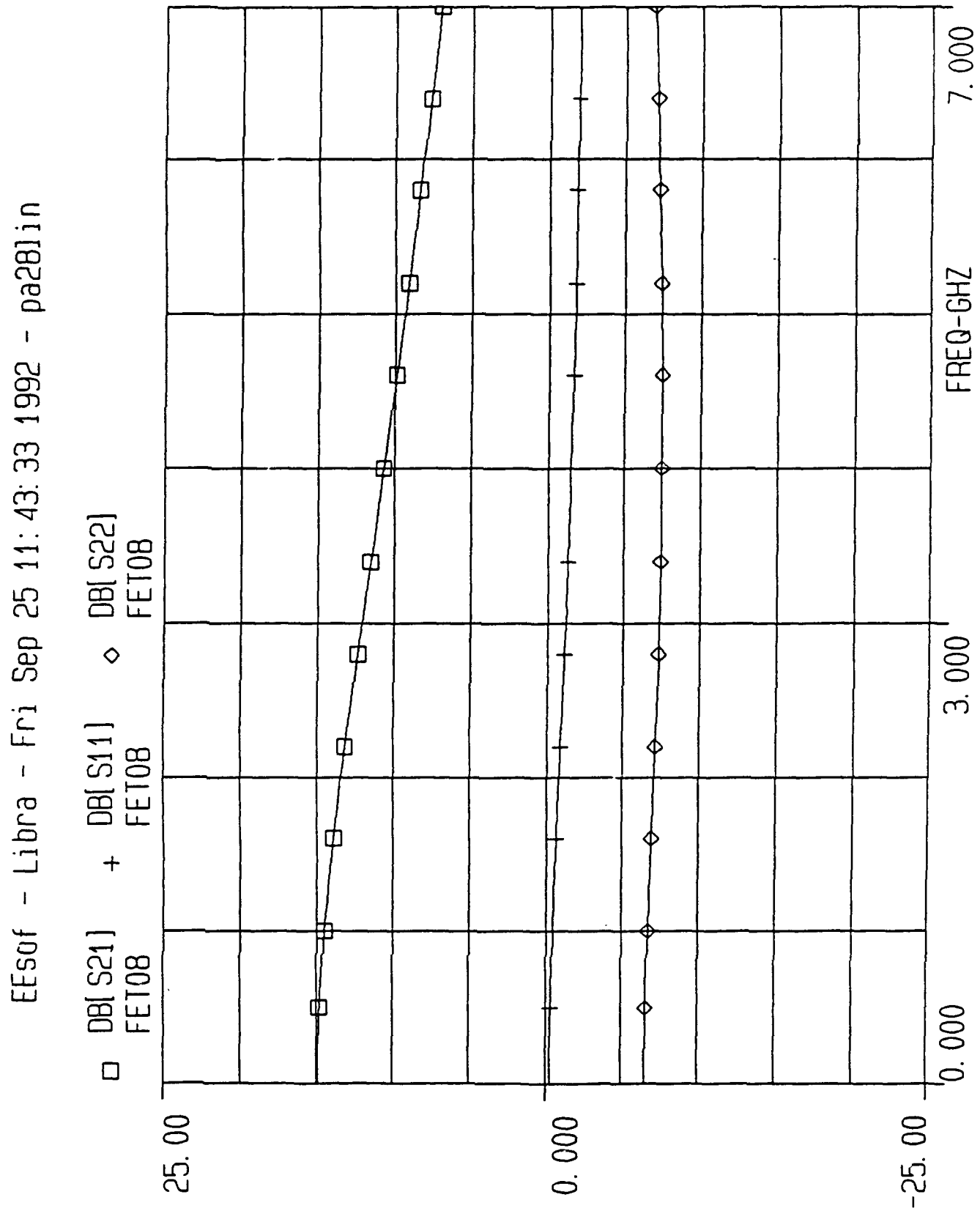
The validation task used these and other device data [10] to put together MMIC models of an LNA and a power amplifier in the frequency range of 1 to 10 GHz for E3 analysis on the SUN work station. This modeling also used Rome Laboratory's new layout software ACADEMY [11] as an adjunct to LIBRA on the work stations.

Several versions of a MMIC power amplifier were modeled using net lists, layouts, schematics, drawings and other device performance data in the literature. Some of these design data had been previously obtained by Rome Lab from ITT, Raytheon, GE, Triquint, Harris, and EEsof. The nonlinear GaAsFET models used are those devised by Rome Lab as described above and in [12], and which were further refined and tweaked for this work.

Shown in figure 4 are linear S-parameters for the baseline power amplifier in the T/R module. It uses a conventional Curtiss-Statz, level 2 model for the FETs. It is very broadband with good gain and is reasonably matched at the signal ports. Shown in figure 5 are the comparable power dependent, nonlinear S-parameters for the same baseline amplifier. It uses a modified Rome Lab (nonlinear) model for the FETs which was derived from the above data.

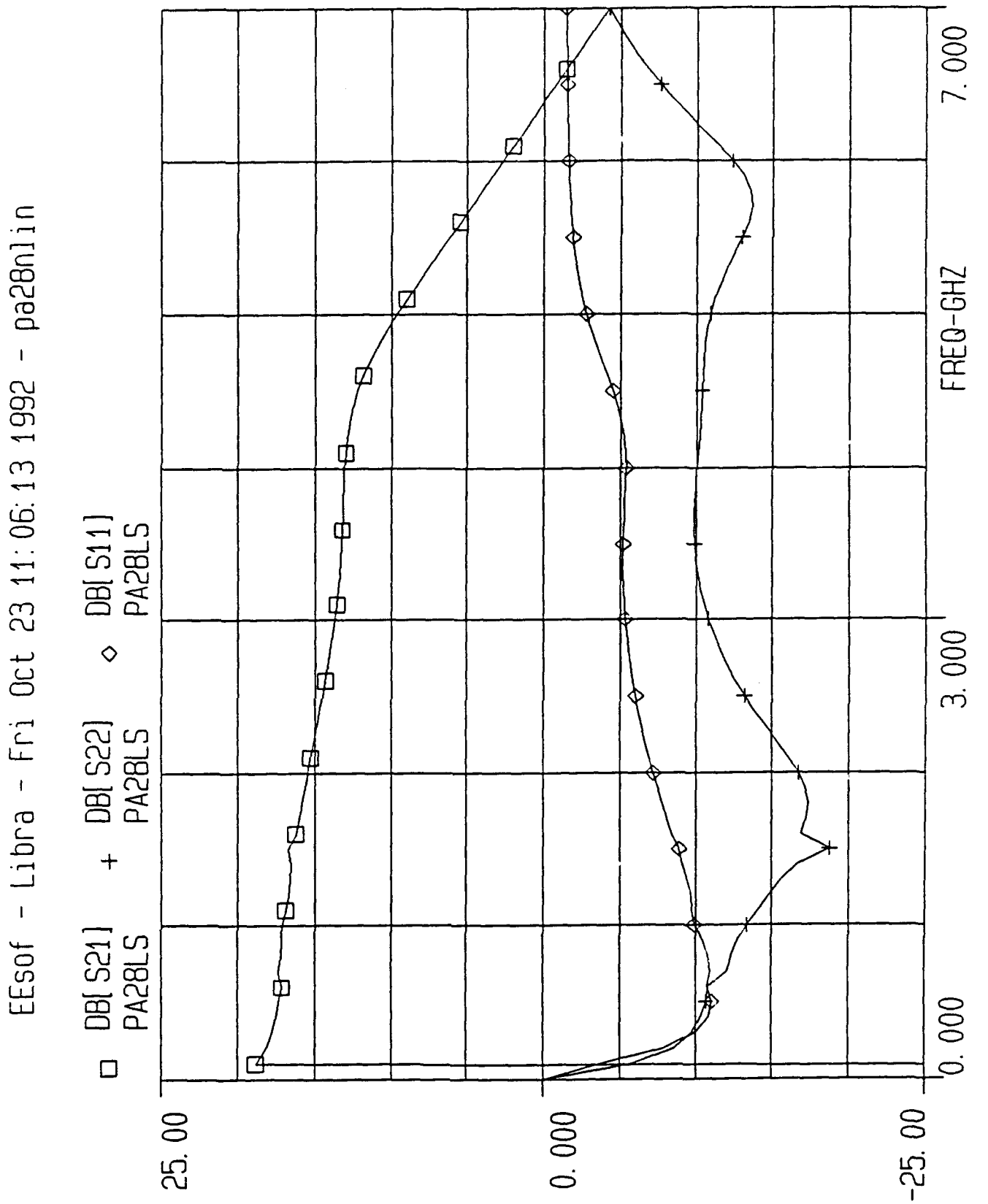
While its gain is still relatively stable and acceptable over the frequency band of interest, insertion loss and mismatch performance are now improved considerably. The data does suggest unexpected resonances at 1.5 GHz and 5.8 GHz. These are some of the typical metrics selected to demonstrate the E3 effects at the desired and undesirable ports.

A considerable effort is required to devise a MMIC model, especially the active microwave FETs. This is related to the lack of good device parameter data which is usually not readily available in the open literature. Many of the device or circuit parameters are measured and guarded as proprietary design data.



Linear Baseline Power Amplifier

FIGURE 4



Nonlinear Baseline Power Amplifier

FIGURE 5

While MMIC performance data attendant with these device parameters are reported in the literature, it is very difficult to replicate them without all the FET parameters and values. This difficulty is especially troublesome when attempting to do the nonlinear models needed for the E3 analyses.

A consequence of attempting this kind of reverse engineering of the baseline MMIC models is time consuming modeling with much "hit or miss" parameter tweaking. With limited FET device parameter data and (MMIC) associated performance data, the E3 modeler is severely handicapped. Simulating E3 interactions in a victim MMIC cannot even begin until a good baseline model of the MMIC is devised and validated. Hence, we were only marginal in obtaining E3 data for the vector model validations.

The conclusion is inescapable: FET device and other microwave circuit parameters must be measured "in situ" for the MMIC of interest. The resulting model predictions for a baseline performance can then be compared with the measured MMIC performance and tweaked accordingly to bring the circuit models into some conformance with the measured data. Appendix C of this report contains a list of MMIC device parameters suggested in a measurements program to actively support MMIC modeling.

The device parameters identified for measurement are taken from the open CAD literature, especially the more noted papers reprinted here for convenience in Appendix B of this report. Here, modeling an active microwave, common source FET begins with the basic problem of finding a suitable relationship between the measured drain-to-source current and the drain-to-source voltage for the family of measured gate-to-source voltages. The parasitic capacitances, gate-to-source, drain-to-source, and the gate-to-drain are formulated as voltage dependent, nonlinear diodes. These are the key issues in FET modeling.

In this task we also considered circuit modeling and topology for possible E3 power drivers for victim MMICs. We postulated Thevenin and Norton equivalent sources to model electric and magnetic field coupling through platform apertures and onto cabling and connectors of the modules and onto the interior microstrip conductors, traces, and substrates of a module. These microwave transmission lines and other traces then in effect can conduct the offending E3 waveforms onto the input ports of the MMICs.

Finding good circuit models and field relatable topologies for the E3 drivers, and especially their functional relationships with external, offending E3 electric and magnetic fields remains of interest. For example, the E3 source impedances and admittances, and their power dependent flux densities at the victim MMIC ports need to be investigated with both frequency and platform dependencies.

This might start with selected (and simple) aperture and cabling geometries to accurately synthesize an equivalent Thevenin and Norton source model. A fields analysis of the platform and its interior might provide the necessary data.

The E3 sources considered here were simple voltage and current dependent power sources that represent the incident E3 field levels and polarizations. Two source configurations were considered and are shown in figures 6 and 7 driving a Lange coupler, singly balanced microwave mixer. A nonlinear Lange coupler was chosen to show the difference in nonlinear effects attributed to the different source configurations used.

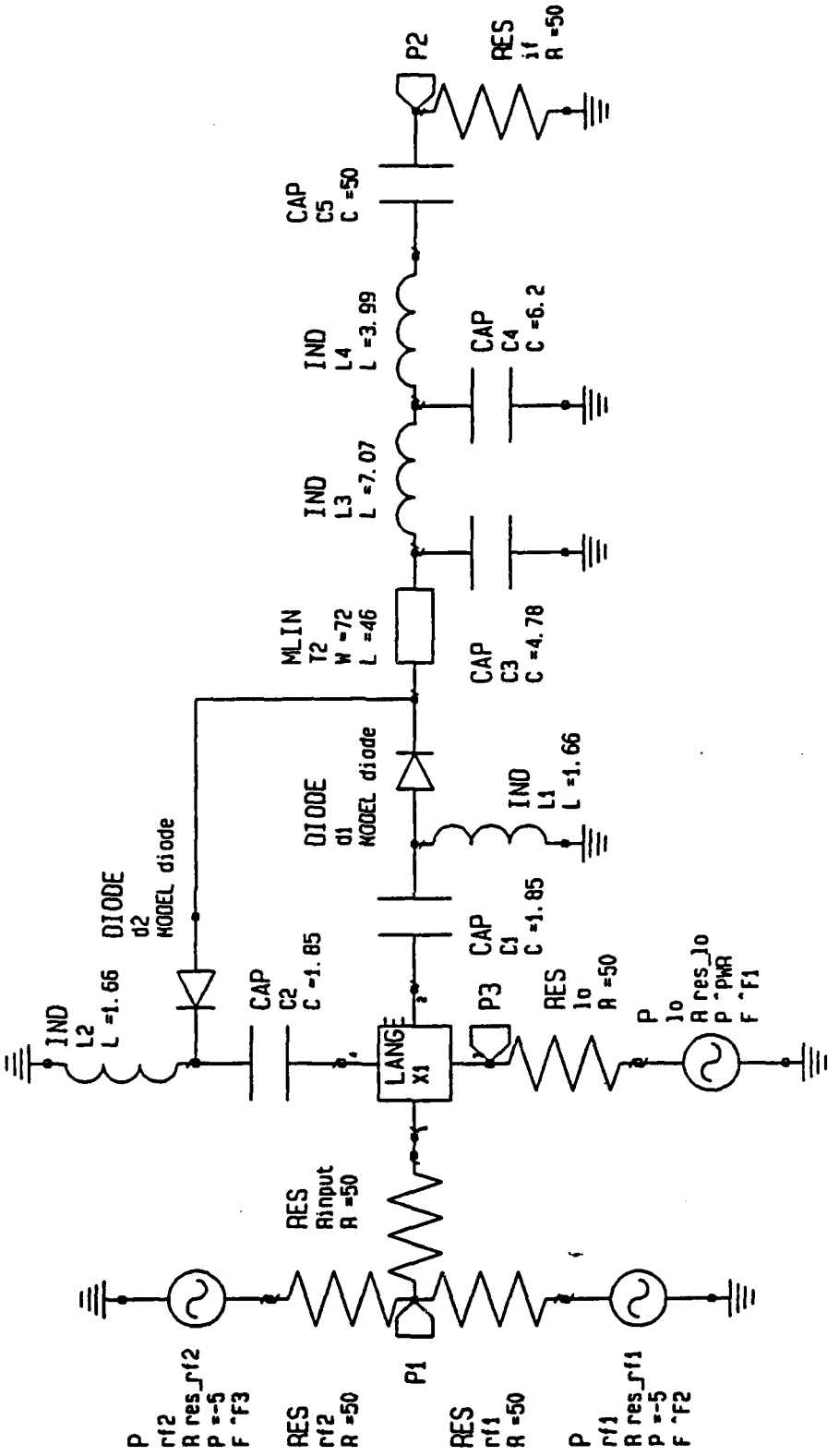
It can be shown that for the parallel and series source configurations in figures 6 and 7, the respective available powers of each source combine additively. This can be seen by first converting the parallel voltage sources to equivalent current sources and then combining the current sources with their generator admittances.

In the case of the series voltage sources, they add directly and deliver their power through their combined generator (series) impedances. The total available power from the series pair is now easily computed. From this, it can be seen that the total available power from either configuration is the same if both power sources are equal. Of course, these results could easily have been deduced from elementary concepts of conservation of energy or power.

While the available E3 powers from each of these sources were set to the same level, and the combined total powers available were also the same for both driver configurations (i.e., the sum of each source), real differences in MMIC responses to the E3 waveforms were noted. For example, in figures 8 and 9, the total actual POWER_IN and the total actual POWER_OUT differ by 3.6 dB and 3.4 dB, for the two source configurations, respectively.

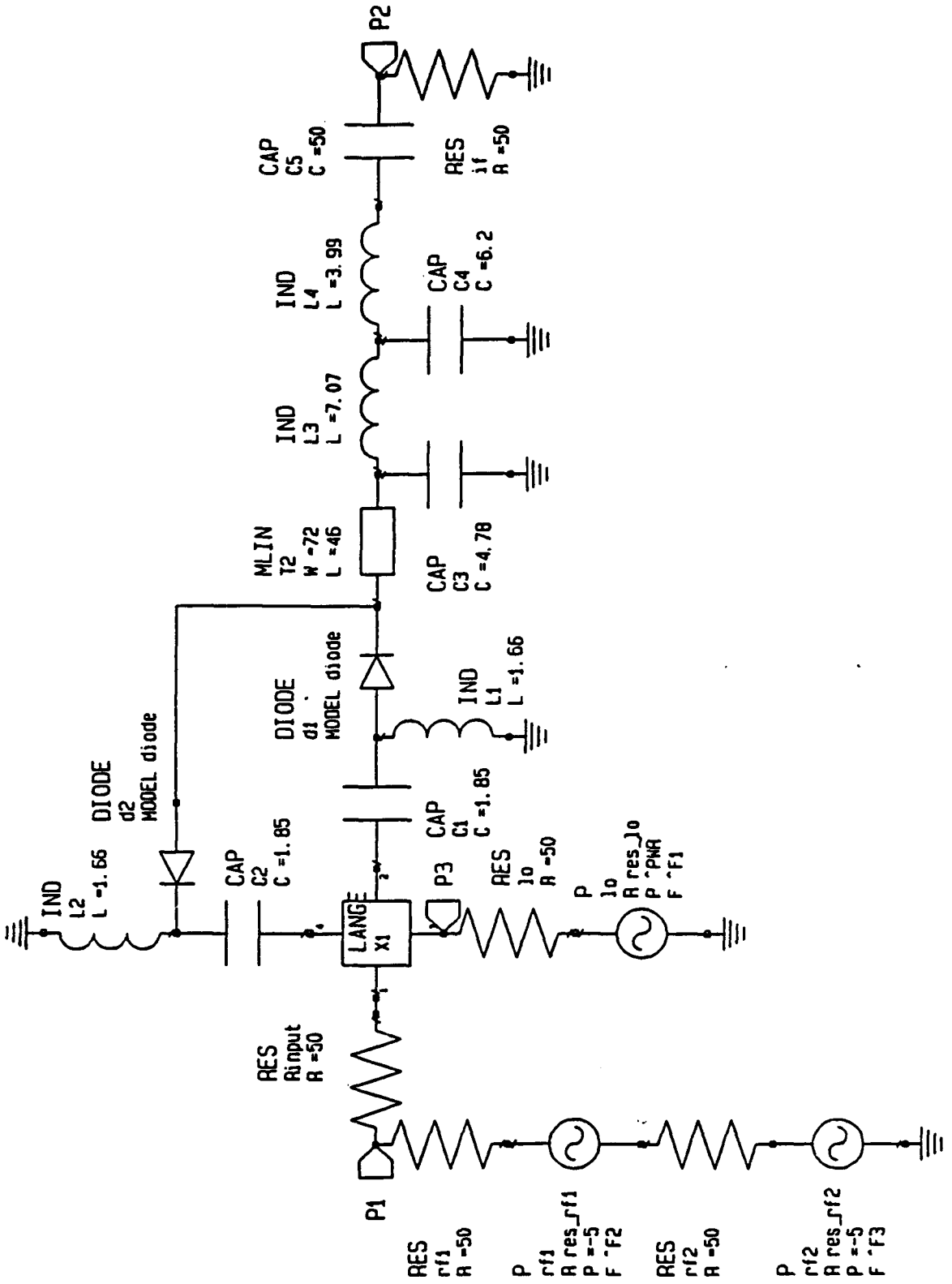
The differences are attributed to mismatched, input impedances of the two different driver source configurations. Such mismatches can easily account for the differences in the respective input powers that were actually delivered from the two configurations of combined sources. This contention is supported with a very simple calculation.

Recall that the combined available powers are sums of their individual available powers for the two configurations. In the more general case with different source impedances, the total available power is a linear combination of each available source power plus another term that is proportional to a product of the individual available powers. These power terms are dependent on the respective source resistances; the linear power terms are simple power dividers, and each different in the two parallel and series configurations.



Lange Mixer With Parallel Sources

FIGURE 6



Lange Mixer With Series Sources

FIGURE 7

testdan.ckt data

** Input Power: 6.00000 dBm **
** Input Frequency: 3.75000 GHz **

FREQ-GHz	SPECOUT MIXER	SPECIN MIXER	POWERIN MIXER	POWEROUT MIXER
0.00000	-230.000	-230.000		
0.05000	-48.2515	-111.235		
0.10000	-27.1364	-90.0365		
0.15000	-26.8138	-83.3936		
3.60000	-84.1895	-42.1921		
3.65000	-86.3115	-44.2637		
3.70000	-82.6103	-45.1518		
3.75000	-66.9094	-0.22547		
3.80000	-76.6947	-38.2780		
3.85000	-76.1286	-11.1377		
3.90000	-76.1735	-11.1379		
3.95000	-82.2044	-58.3687		
4.00000	-83.3165	-46.8066		
4.05000	-85.8015	-50.2411		
7.50000	-92.9021	-33.4431		
7.60000	-107.931	-35.7839		
7.65000	-108.259	-35.9333		
7.70000	-113.017	-50.0563		
7.75000	-109.094	-60.0772		
7.80000	-115.726	-59.2225		
11.2500	-117.562	-35.2781		
11.3500	-111.621	-38.1986		
11.4000	-112.963	-38.6286		
11.4500	-125.610	-47.7233		
11.5000	-127.787	-45.8503		
11.5500	-117.256	-39.8186		
11.6000	-129.708	-51.1545		
11.6500	-117.755	-40.8834		
11.7000	-125.849	-47.6928		
Tot Pwr			0.43537	-23.9453

Lange Power Spectra: Parallel Sources

FIGURE 8

x3tone.ckt data

** Input Power: 6.00000 dBm **
** Input Frequency: 3.75000 GHz **

FREQ-GHz	SPECOUT MIXER	SPECIN MIXER	POWERIN MIXER	POWEROUT MIXER
0.00000	-230.000	-230.000		
0.05000	-60.3683	-112.657		
0.10000	-31.1979	-94.2129		
0.15000	-31.5539	-87.5919		
3.60000	-83.8119	-48.9389		
3.65000	-84.5532	-49.6704		
3.70000	-86.3645	-44.0454		
3.75000	-72.6575	3.89849		
3.80000	-95.5587	-46.9791		
3.85000	-79.7173	-13.1478		
3.90000	-81.0041	-13.1504		
3.95000	-81.5302	-41.3861		
4.00000	-87.1484	-44.4562		
4.05000	-89.2120	-46.7956		
7.50000	-95.7596	-35.7551		
7.60000	-125.338	-36.2807		
7.65000	-122.358	-36.3973		
7.70000	-112.529	-48.9340		
7.75000	-112.280	-62.4038		
7.80000	-122.588	-53.4613		
11.2500	-117.644	-30.8442		
11.3500	-117.181	-45.4218		
11.4000	-117.581	-42.9829		
11.4500	-133.441	-45.9738		
11.5000	-128.638	-44.6591		
11.5500	-118.970	-37.7743		
11.6000	-134.112	-57.5220		
11.6500	-118.621	-40.0739		
11.7000	-135.720	-55.8939		
Tot Pwr			4.07035	-28.3589

Lange Power Spectra: Series Sources

FIGURE 9

The above results are shown in figures 10 and 11 where the total available powers are plotted against the mismatch ratio R1/R2 for real impedances for parallel and series voltage sources. With an available power of -5 dBm fixed from one source, the plot shows a six-fold family of curves of available powers from the other source, ranging from equal power to six times the -5 dBm source.

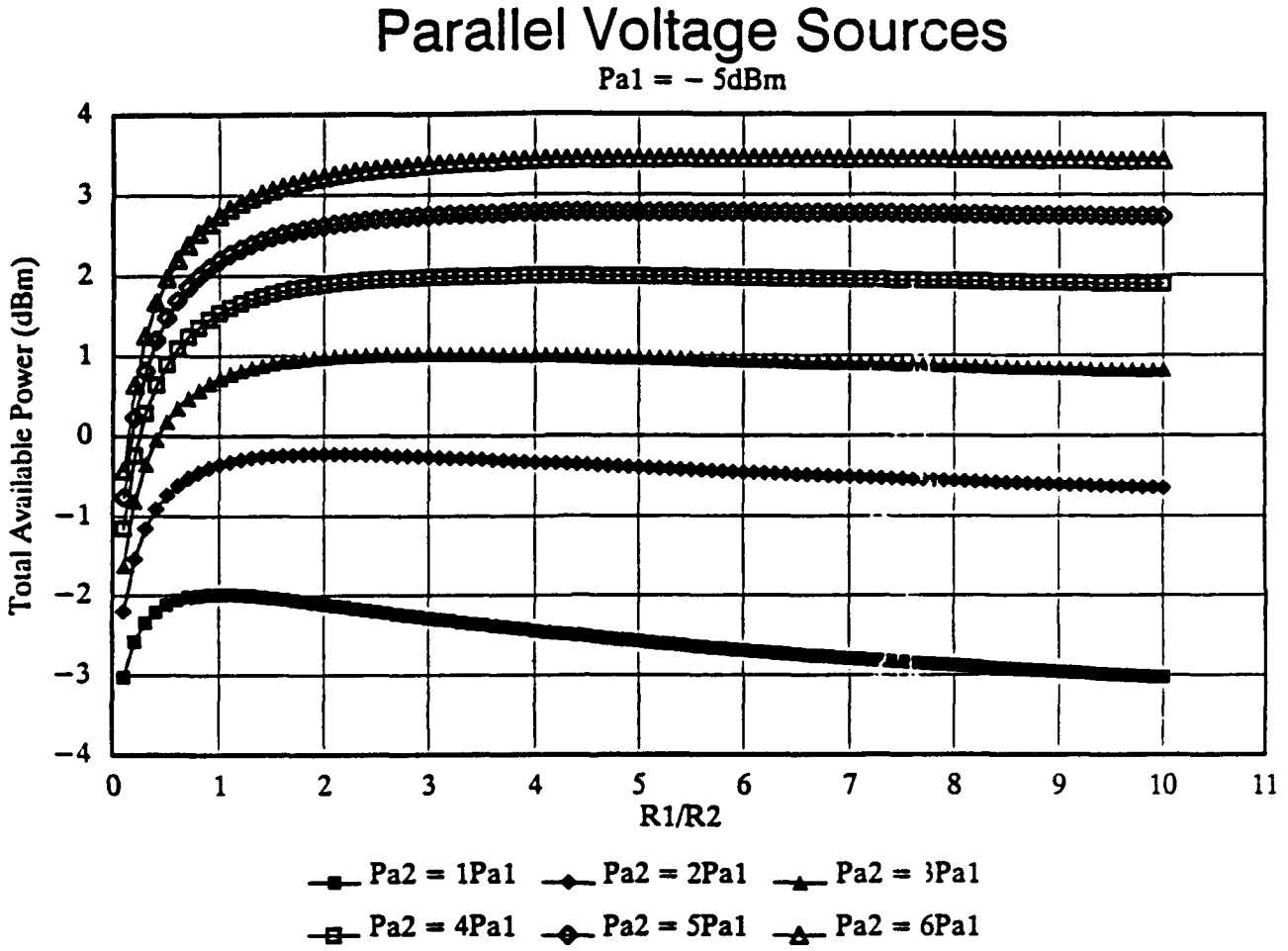
Note that when the available powers of each source are each equal to -5 dBm, the total available power from the combined pair is -2 dBm or just doubled as expected. Next, note that as the respective powers from each of the sources differ by ratios of 1 to 6, their combined powers behave as shown. These parametric curves indicate that peaks occur when the ratio k (=R1/R2) = 1, 2, 3, ... 6 for the parallel case and when k= 1, 1/2, 1/3, ...1/6 for the series case. These are then the design ratios needed to match the real impedances of the combined pairs for a maximum power transfers.

Before leaving the issues of FET modeling, it may be of interest to consider the major GaAsFET models available today and which are used extensively throughout the industry. They are the six models given in Appendix B and they are the most widely cited in the design trade. As discussed before, the functional relationship between the drain-source current and the drain-source voltage, the common source FET transfer function, is a key design driver for large signal FET models.

Figures 12-17 show some of these typical transfer functions for the common source configuration with gate-source voltages (Vgs) which range from -1.2 V to 0.2 V. These GaAsFET models differ from each other in the ways the author choose to model the channel currents; i.e., Curtice's quadratic and cubic functionals, and Materka's modified exponential functionals, and the functionals used by Statz, Tajima, Gopinath, et al.

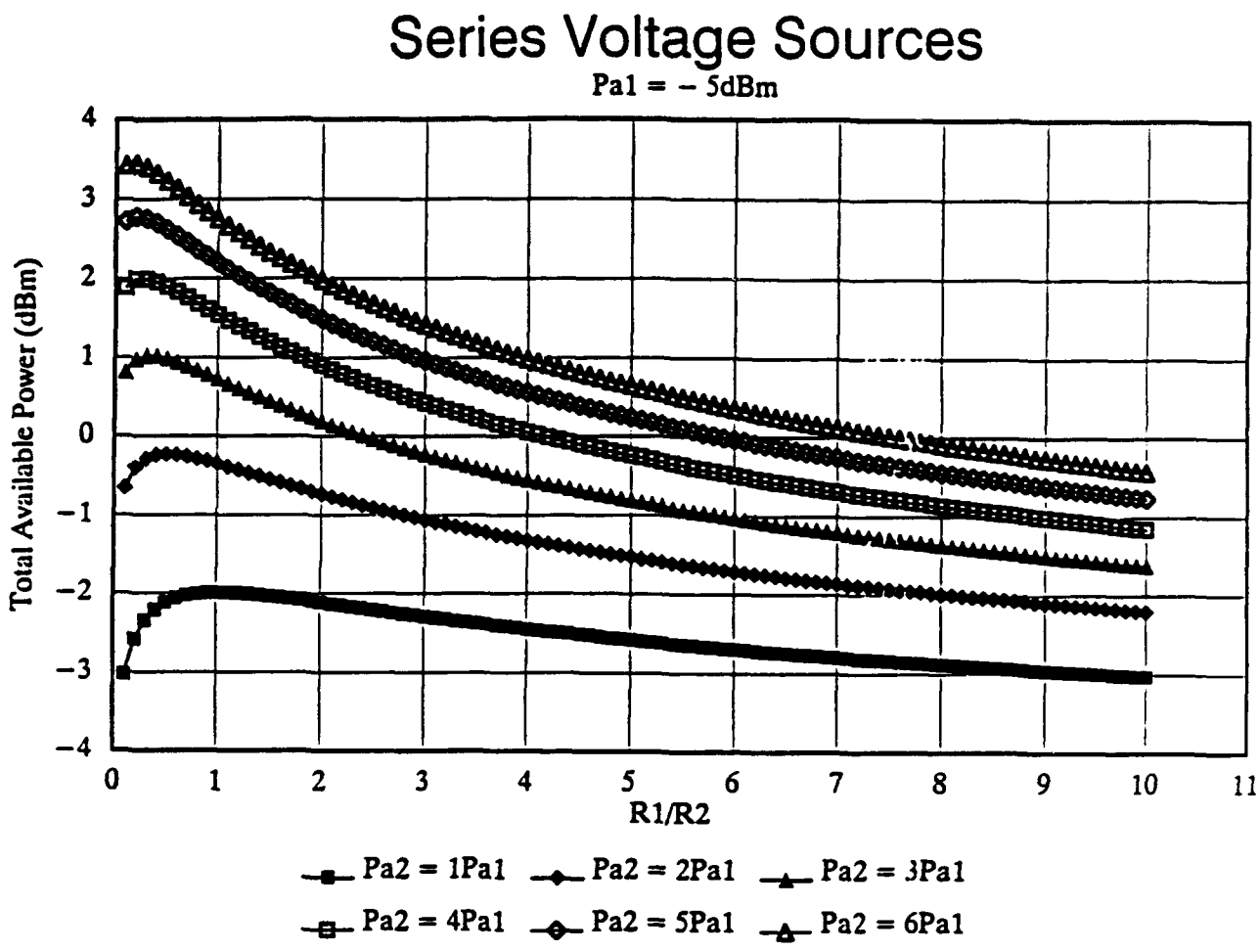
Figures 18-23 show approximate comparisons of these important GaAsFET models at fixed values of Vgs over the same ranges as above. Device parameters used to compute each of these transfer functions were approximately the same. They were selected from the above papers and from data available in LIBRA documentation. Note the good agreement among these curves, at least for this particular set of FET device parameters chosen for this comparison.

The design merits and trade-off benefits attendant with any particular functional model and its description would, of course, require careful review of the papers in Appendix B, supplemented with good measurements data.



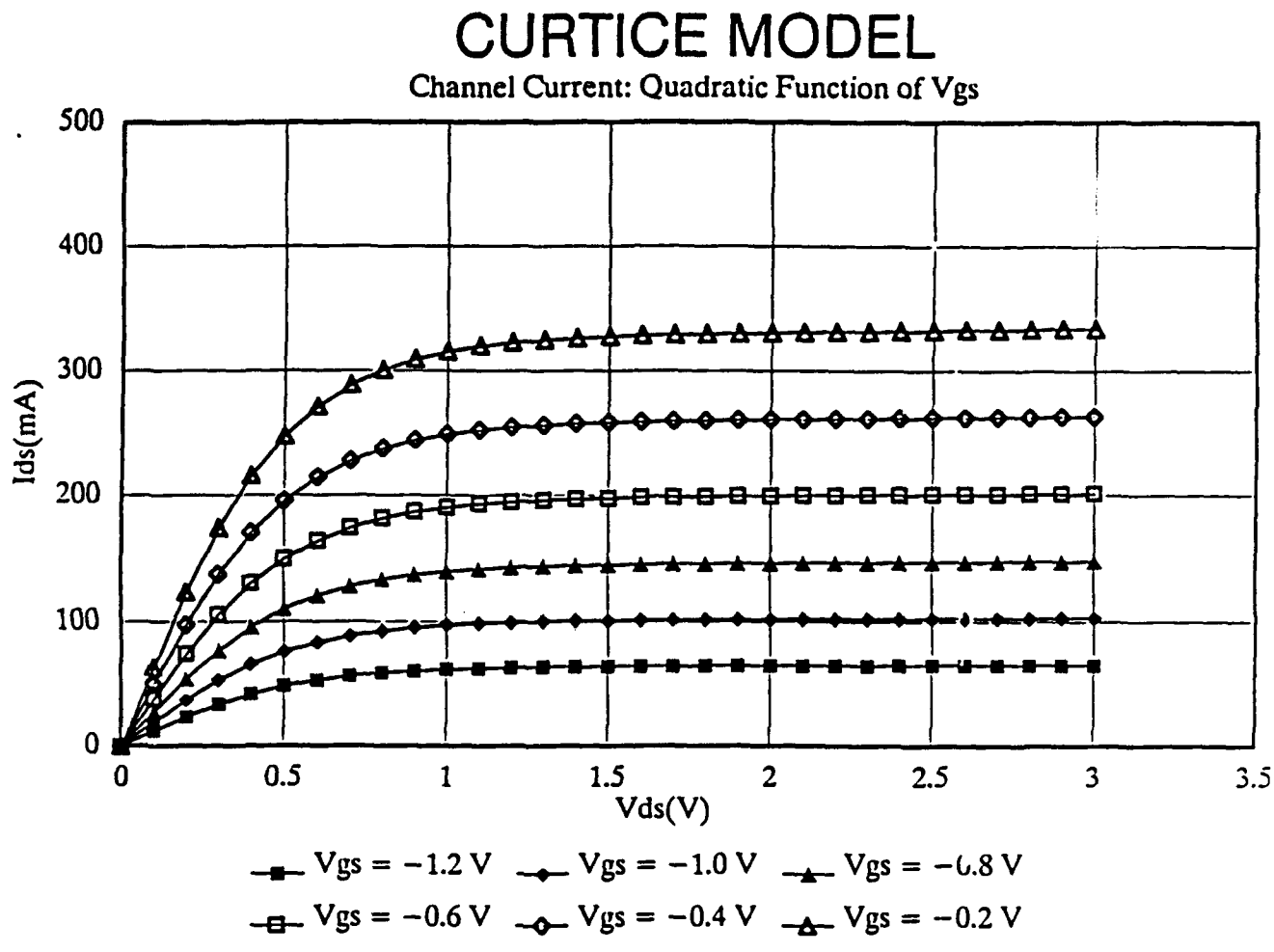
Available Power From 2 Parallel Sources

FIGURE 10



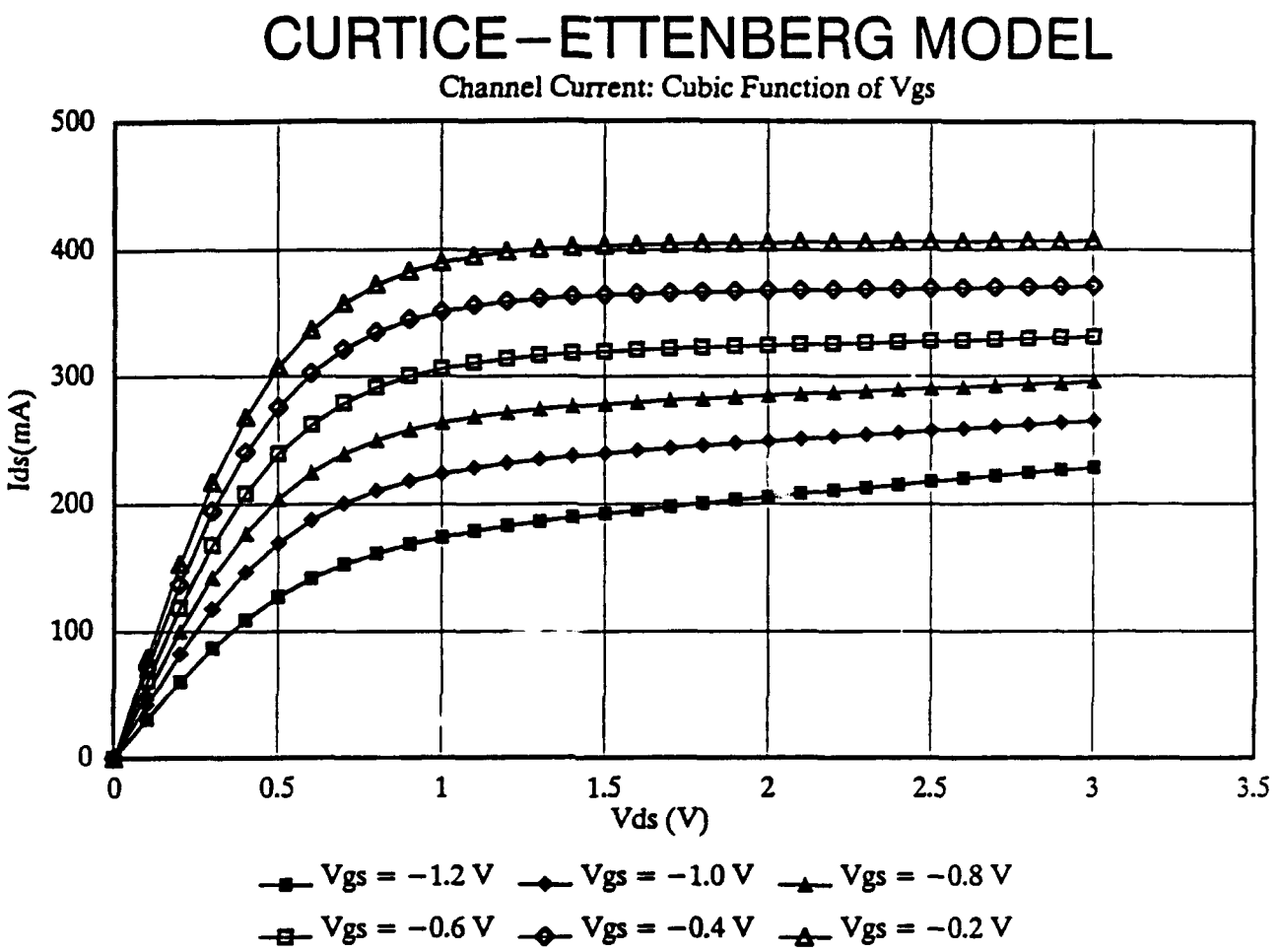
Avaialable Power From 2 Series Sources

FIGURE 11



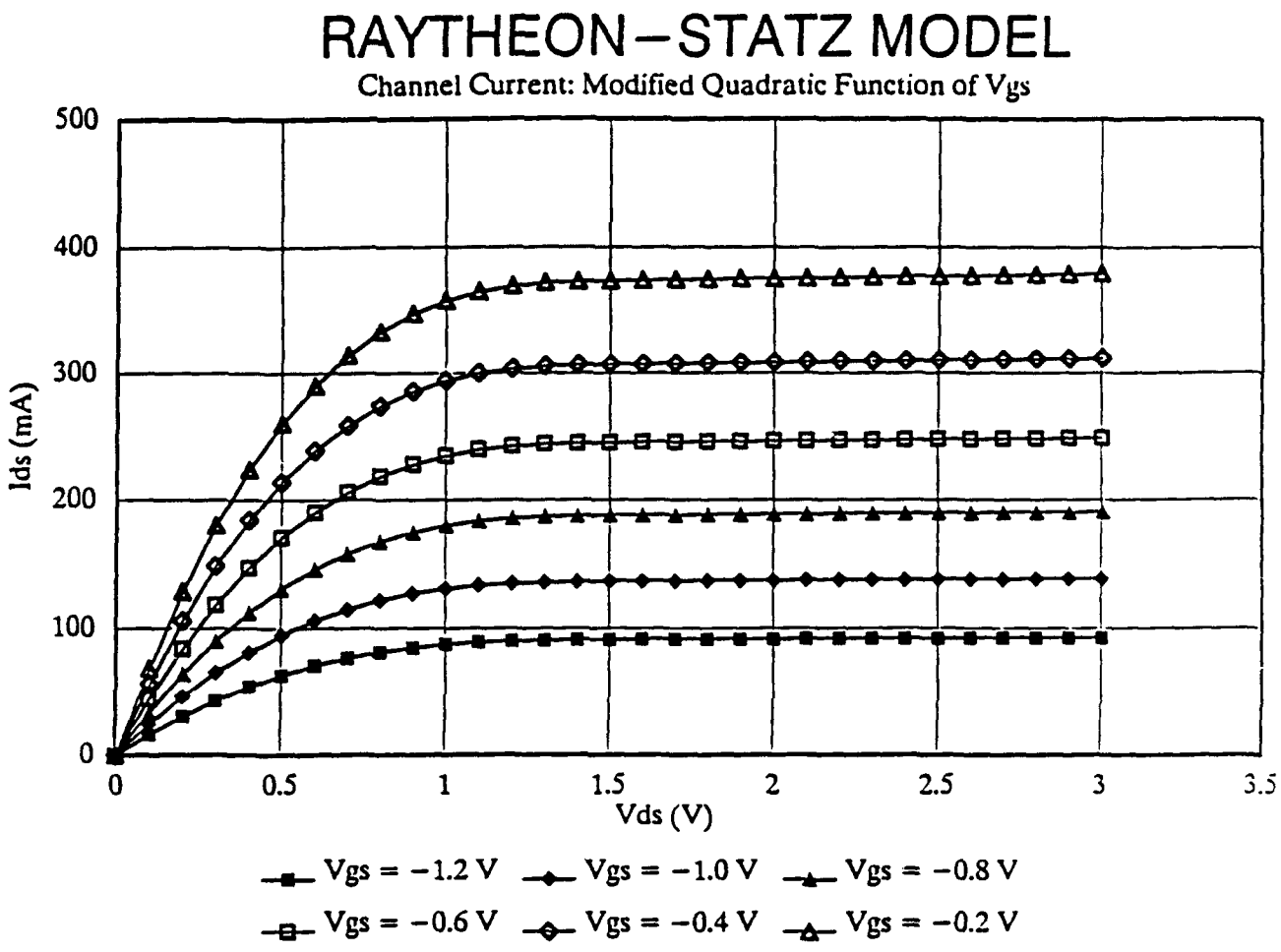
Curtice MESFET Model

FIGURE 12



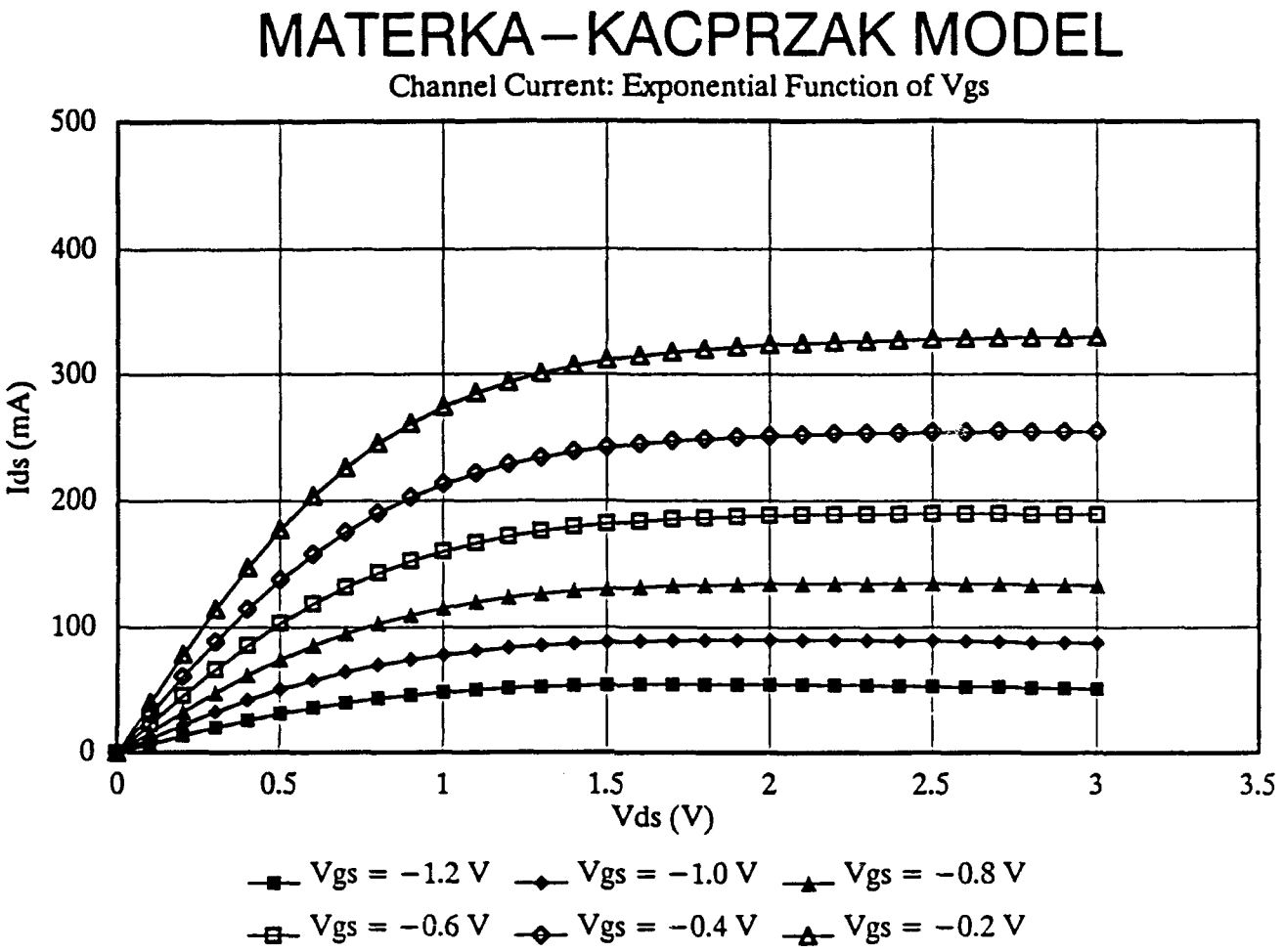
Curtice-Ettenberg GaAs FET Model

FIGURE 13



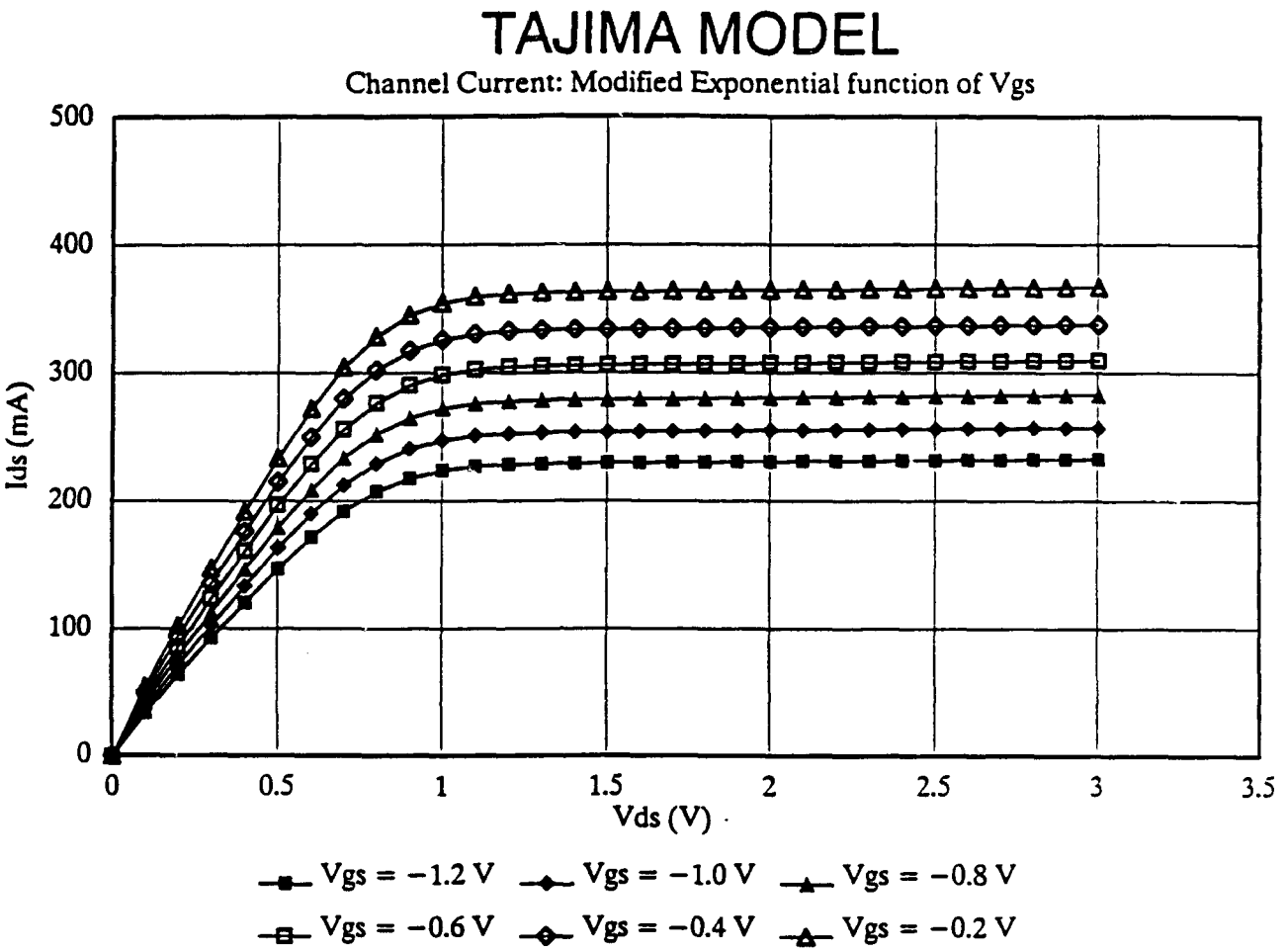
Raytheon-Statz GaAs FET Model

FIGURE 14



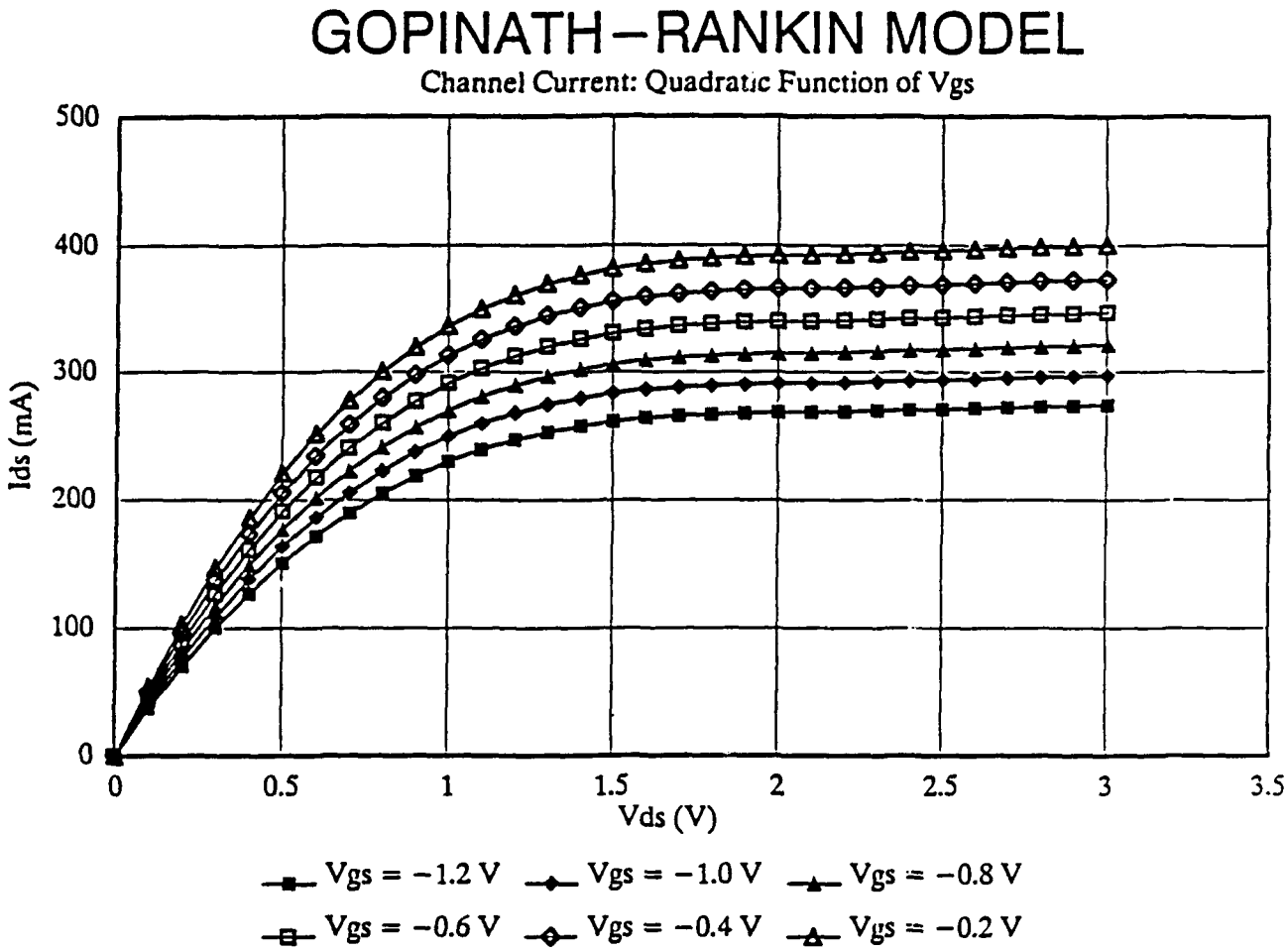
Materka-Kacprzak GaAs FET Model

FIGURE 15



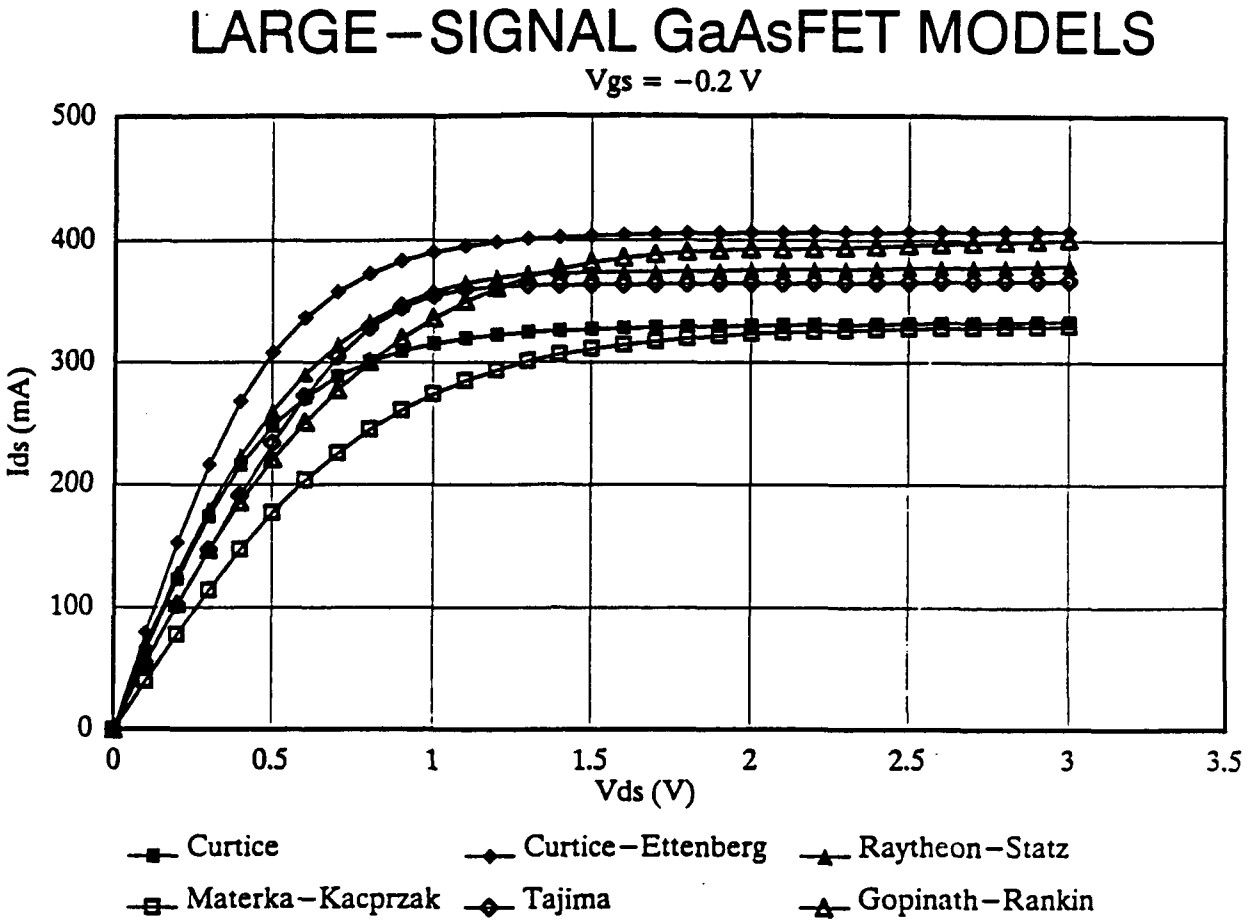
Tajima GaAs FET Model

FIGURE 16



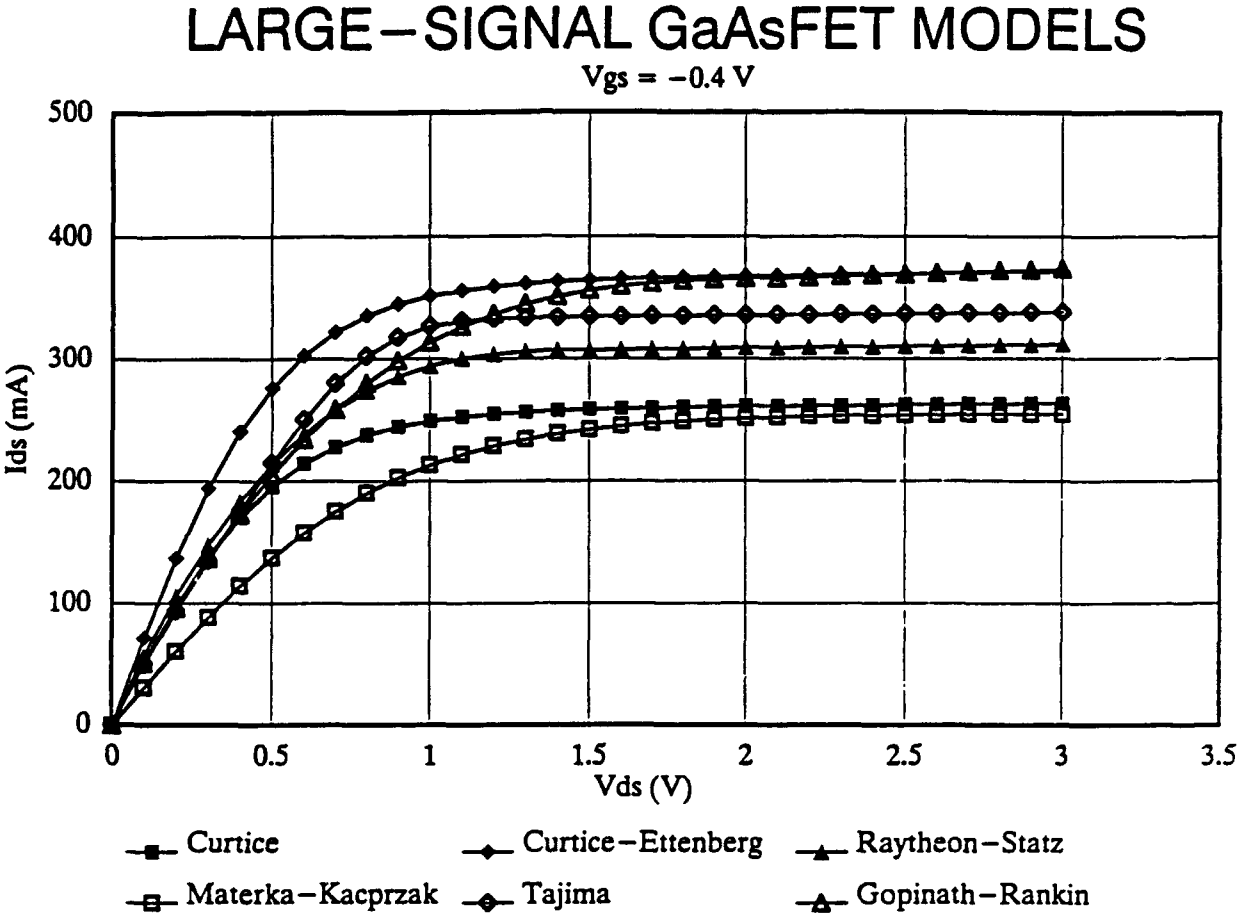
Gopinath-Rankin MESFET Model

FIGURE 17



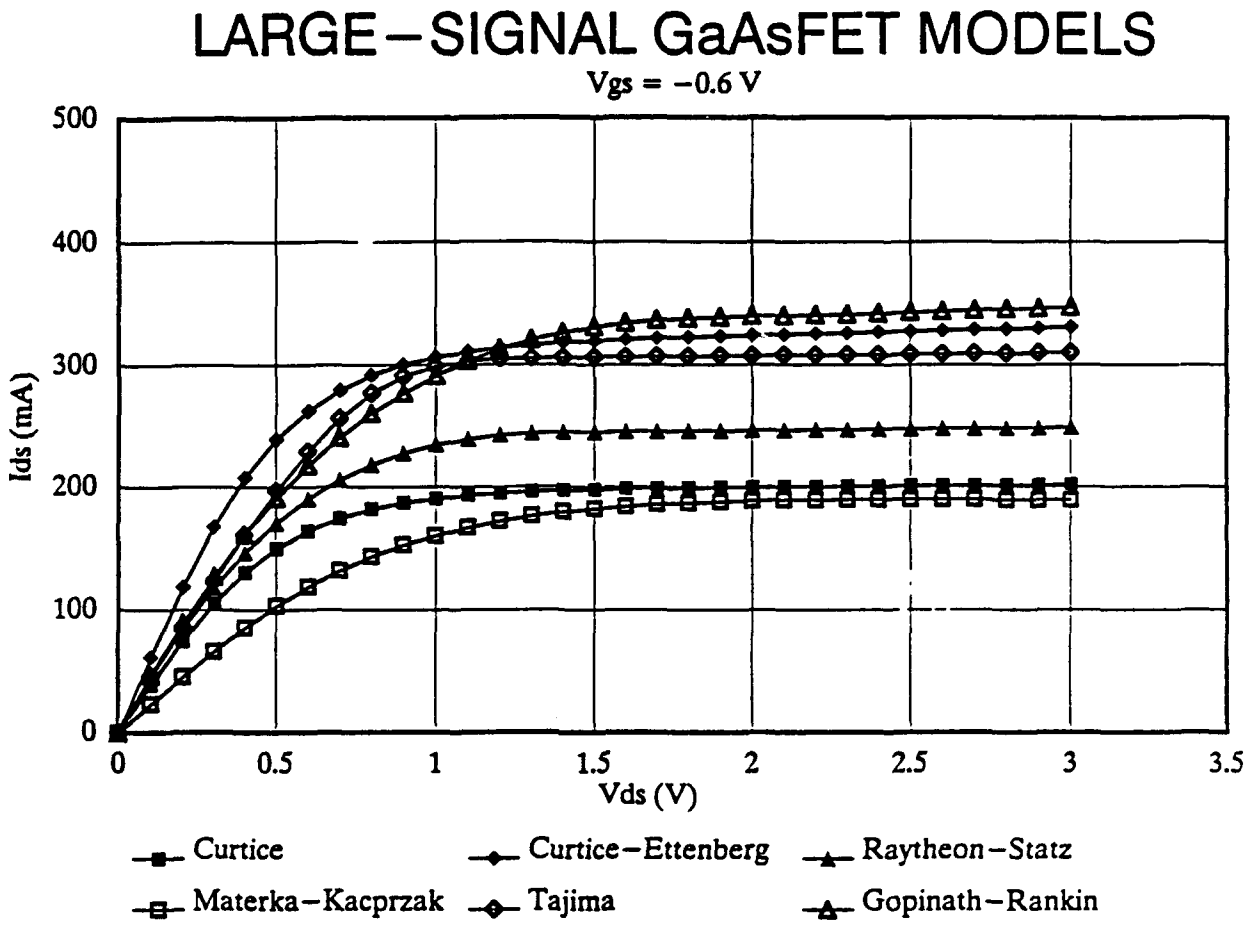
Comparative Models: Vgs = - 0.2 V

FIGURE 18



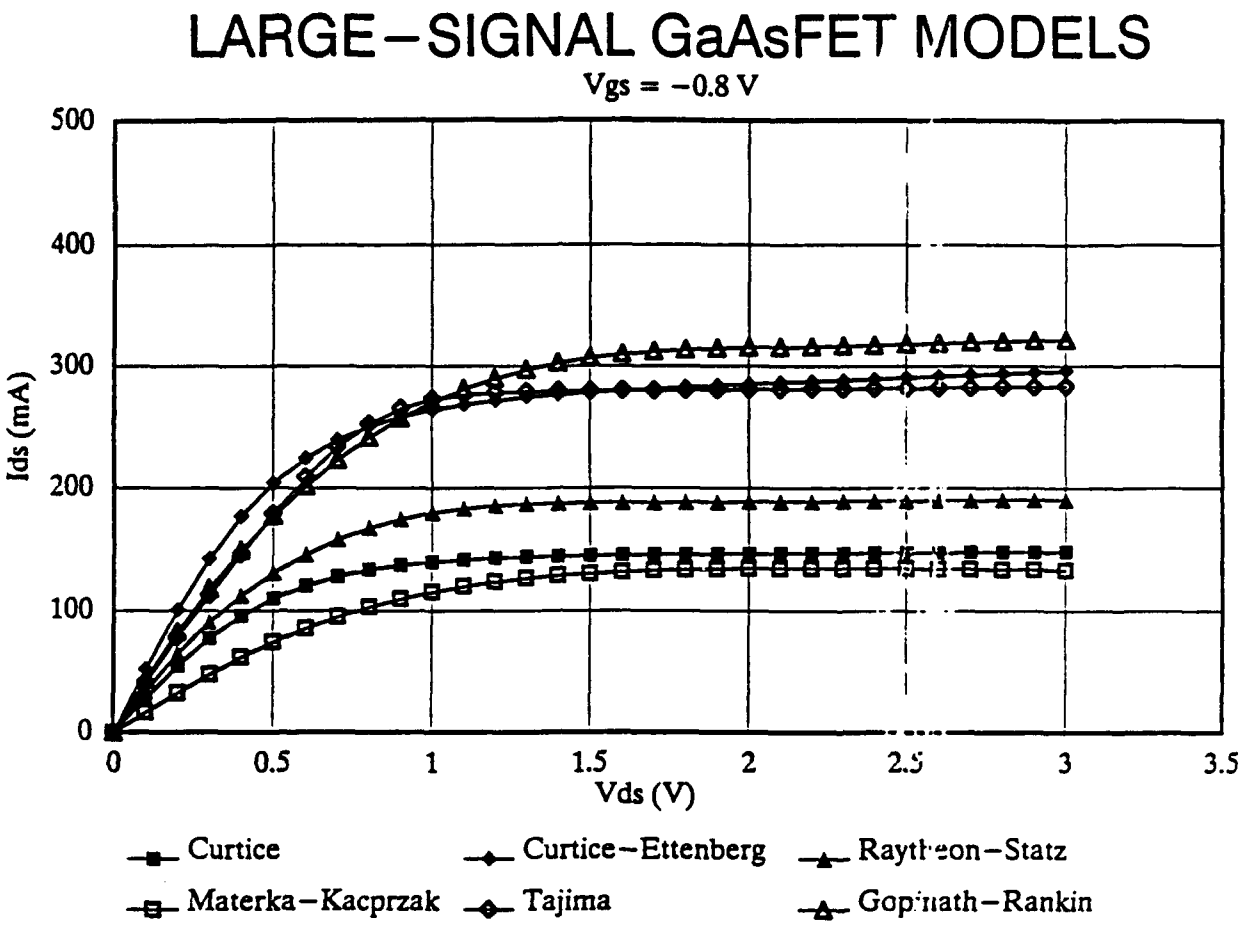
Comparative Models: Vgs = - 0.4 V

FIGURE 19



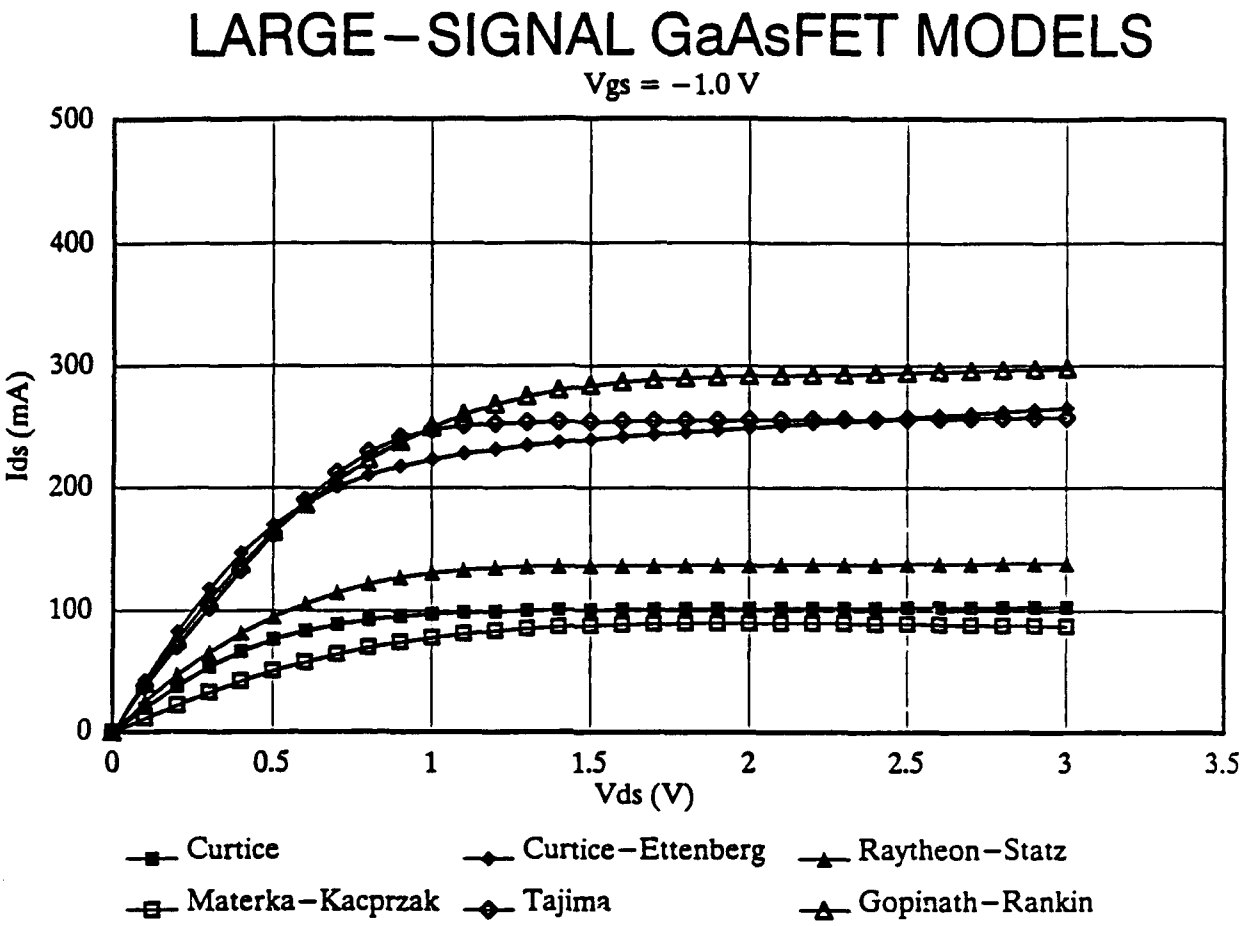
Comparative Models: Vgs = – 0.6 V

FIGURE 20



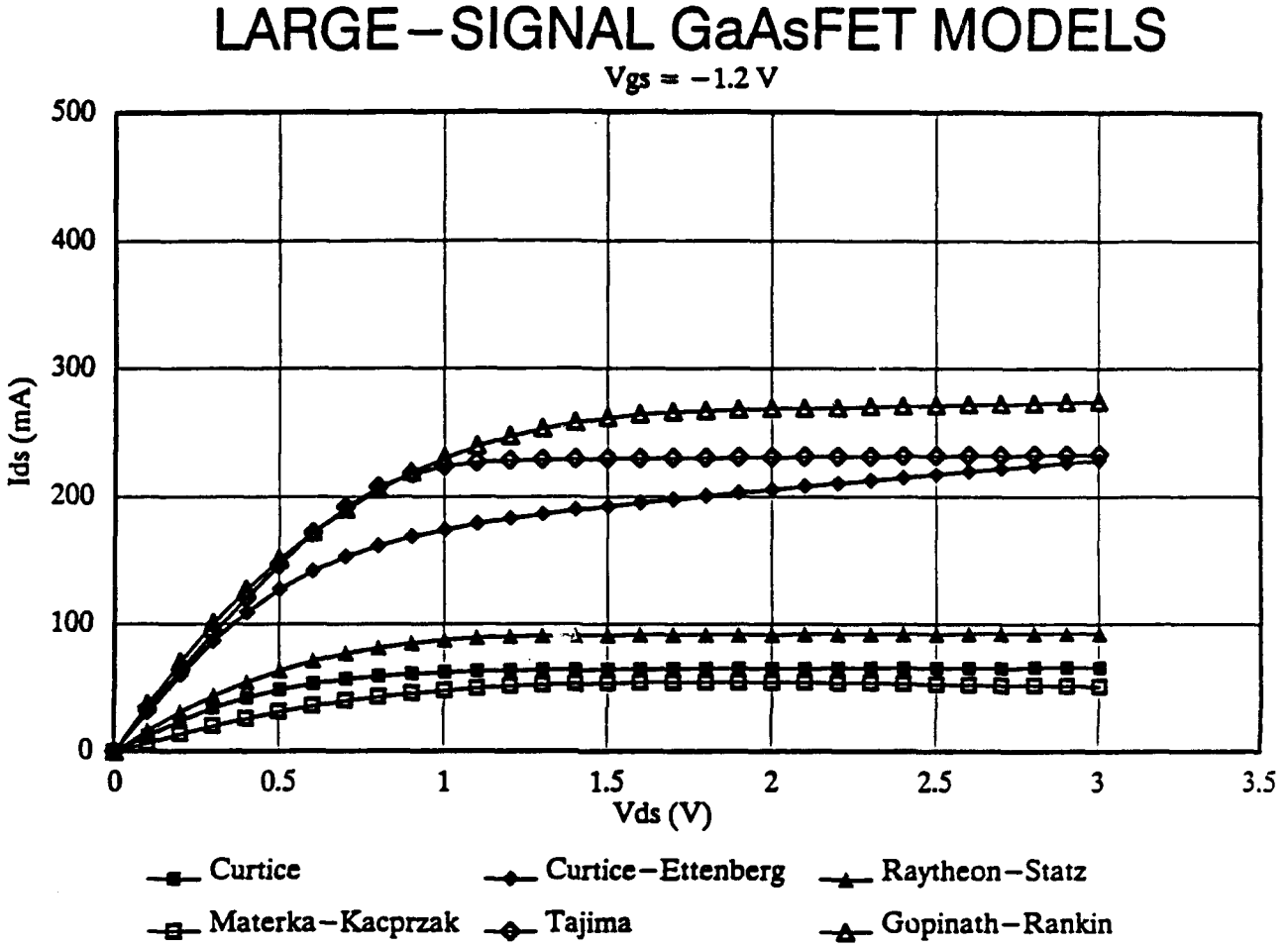
Comparative Models: Vgs = - 0.8 V

FIGURE 21



Comparative Models: Vgs = - 1.0 V

FIGURE 22



Comparative Models: Vgs = - 1.2 V

FIGURE 23

TASK 4 - DESIGN PLANS

Design plans developed for this task contain approaches to E3 modeling with special emphasis on the (E3) related parameter measurements for the MMICs and T/R modules of interest. A brief plan to define or specify the electromagnetic environments for victim platforms is also included. In addition, these plans contain approaches to modeling and measuring E3 susceptibilities of the newly emerging packaging technologies of MCM, multi-chip modules.

These plans (and those in appendix A which also contain suggested program recommendations) cover some E3 issues related to integrated test diagnostics technologies. These new issues are especially those E3 related effects which may be unintentionally "enhanced" by designing in or incorporating BIT, BIST and boundary scan, test circuit cells into the host circuits and modules for improved testability.

The three design plans included in the following pages are:

a) "Some Circuit Parameters Required for CAD Modeling and Analysis of E3 in MMICs"

b) "Defining an Electromagnetic Environment for Predicting T/R Module Susceptibility"

c) "Design areas in T/R modules of Concern to E3 in MMICs"

An extensive literature search on nonlinear circuits modeling was completed in the course of developing the design plans. Most of the reference searches were done with the excellent assistance and considerable assets of the Rome Laboratory Technical Documents Library. The end product is the large bibliography that is included elsewhere in this report. This very current bibliography also contains some excellent sources of theoretical material relevant to the n-dimensional polynomials used for the advanced classical modeling.

SOME CIRCUIT PARAMETERS REQUIRED FOR CAD MODELING AND ANALYSIS OF E3 IN MMICs

Microwave Integrated Circuit Parameters

The microwave circuit parameters which are used to model MMICs are user inputted data to CAD software programs like SUPERCOMPACT, TOUCHSTONE, MICROWAVE SPICE, and LIBRA. These parameters are attributes (or, characterizations) of both the active devices and the passive, transmission line structures used in MMIC models. They provide the numerical values of the circuit elements in the computer models that are used to "mimic" or simulate microwave function(s) and the associated circuitry in the MMIC of interest.

The term "device" is defined here as a packaged entity which performs a single microwave circuit function such as a two stage, low noise pre-amplifier or a four stage, power amplifier. The packaged MMIC device will usually contain one or more active, semiconductor chips (usually, GaAs FETs) mounted and wired together on appropriate ceramic substrates.

In addition, there will also be the associated transmission lines on both chip(s) and substrates to provide the necessary coupling and tuning elements for realizing the particular microwave circuit function. Finally, there are the biasing and ground rails with capacitive and inductive, RF bypass filters.

The device parameters are normally measured but in some cases may also be computed from the device physics. This involves formulating and solving some very basic and complex linear and nonlinear, partial differential wave equations and diffusion equations with more often than not, time varying boundary conditions.

This sort of theoretical approach to device modeling is best left to the device physicists. We recommend an empirical approach to measure the necessary circuit parameters required for CAD modeling and analysis software as user input data.

Measurement Ports

The parameters seem to fall into two categories; those measured externally at the ports of the packaged MMIC and those measured internally at IC and other nodal ports. These latter involve delidding the MMIC package, depassivating the chip(s), etc., in an inert environment to make probe measurements of the GaAs FET's and the passive microwave circuitry contained on/in the chip. We call these two categories of port measurements as external port and internal node measurements, respectively; or simply "external and "internal" ports for short.

The following lists of parameters were compiled from LIBRA and TOUCHSTONE documentation. In addition, available circuit files on the LNA's and PA's for both Rome Laboratory T/R module work and the MMIC DARPA/DoD initiative work which provided by Raytheon were also used. Some of these files contained netlist and layout data parameters for circuit designs and use SUPERCOMPACT, offering a possible perspective on a CAD program different than either LIBRA and TOUCHSTONE.

In addition, the parameters identified are for both the baseline and E3 modeling requirements. The "baseline" refers to those data required to model the MMIC's design-to-performance, the so-called intended functional design. The "E3" modeling requirements refer to those data parameters that are used to characterize the deviations from the baselines. These latter are usually the interference effects.

For example, the third order power intercept is measured in -dBm's of input power as a function of the output power. It is a common characteristic of an amplifier going into 1 dB of saturation (in its output power) because of nonlinear mixing effects in the amplifier which is caused by the E3 power at the input port. This 1 dB level below saturation is considered a practical (upper) limit on the dynamic range and anything less is treated as a deviation from the desired baseline performance.

I. BASELINE MEASUREMENTS: EXTERNAL PORTS

PARAMETER	SYMBOL	COMMENTS
Complex input reflection coefficient	S11	small signal, bias independent
Complex forward transfer coefficient	S21	small signal, bias independent
Complex reverse transfer coefficient	S12	small signal, bias independent
Complex output reflection coefficient	S22	small signal, bias independent
Large signal S parameters	S11, S21 S12, S22	power dependent bias dependent
Noise Figure and other noise related parameters	N.F.	bias dependent
Dynamic Range	DR	bias dependent
DC/RF Efficiency	eta D.C.	RF pwr/DC pwr in bias dependent
Power Added Efficiency	eta A	(RFin-RFout)/DC pwrs; power and bias dependent
Pkg Resonance Factors	Q1, Q2, Q3, etc.	inband and out-of-band, bias dependent
Pkg Q Frequencies	Fr1, Fr2, etc.	bias dependent
Fixture and connector embedding parameters	S parameters, as appropriate	bias dependent, large and small signal dependent

II. BASELINE MEASUREMENTS: INTERNAL NODES

BJT PARAMETER	SYMBOL	COMMENTS
Current gain, Beta	B	Magnitude @ D.C.
Current gain, Alpha	A	Magnitude @ D.C.
Phase Angles	phi sub B phi sub A	Beta Alpha
Time Delays	Tau sub B Tau sub A	Beta delay ps Alpha delay ps
Bandwidth, alpha control	Delta F sub A	3 dB frequencies
Bandwidth, beta control	Delta F sub B	"....."
Collector capacitance	CC	Picofarads
Collector conductance	GC	Siemens (or mho)
Base resistance	RB	Ohms
Base inductance	LB	Nanohenries
Emitter capacitance	CE	Picofarads
Emitter resistance	RE	Ohms
Emitter inductance	LE	Nanohenries
Emitter lead inductance	REL	Nanohenries

FET PARAMETER	SYMBOL	COMMENTS
Transconductance	G	Siemens (or mho)
Time delay	T	transconductance
Roll-off frequency	F	GHz, MHz, kHz, etc.
Roll-off Slope	Delta G/delta F	dB/octave
Gate/Source capacitance	CGS	Picofarads
Gate/Source conductance	GGS	Siemens (or mho)
Channel resistance	RI	Ohms
Drain/Gate capacitance	CDG	Picofarads

Drain/Source capacitance	CDS	Picofarads
Drain/Source resistance	RDS	Ohms
Dipole layer capacitance	CDC	Picofarads
Source resistance	RS	Ohms
Gate resistance	RG	Ohms
Noise parameters	P,R,C,Kr,Kg,Kc K1,K2,K3,K4,K5	LIBRA referenced
Drain/Source voltage	Vds	chip bias, volts
Gate/Source voltage	Vgs	chip bias, volts

III E3 MEASUREMENTS: EXTERNAL PORTS

PARAMETERS	SYMBOL	COMMENTS
Harmonic Distortion	User Option	all signal ports all in/out pairs
Intermodulation Distortion	User Option	"
Crossmodulation Distortion	User Option	"
Desensitization	User Option	"
Gain Compression	User Option	"
Gain Expansion	User Option	"
Nth Order Intercepts	P13,P15, etc.	for N=3, 5, etc. bias dependent
E3 Vector Distortion*	User Option	at all the port pairs in all the combinations of any accessible ports including bias, grnd, and digital ports

* "E3 Vector distortion" in an operating multi-port device is defined as the response at any port in which a deviation from its baseline performance is caused by E3 as a source vector connected to any other port. "Baseline performance" of a device is defined as its measured normal operating parameters or the "designed-to" specifications of the device. "Admissible ports" are all the accessible ports or pin pairs on the device package when operating as intended.

Even and odd mode impedances	Z sub e Z sub o	coupled lines
Even and odd mode dielectric constants	K sub e K sub o	coupled lines
Even and odd mode attenuations	A sub e A sub o	coupled lines
Coupler length	L	coupled lines
Lossy capacitor	CAPQ	discrete element
Quality factors	Q sub C Q sub L	discrete C discrete L
Lossy inductor	INDQ	discrete element
Bias voltage supply	Vdd	pkg port (pins)
Bias current drain	Idd	pkg port (pins)

DEFINING AN ELECTROMAGNETIC ENVIRONMENT FOR PREDICTING T/R MODULE SUSCEPTIBILITY: A DATA ACQUISITION PLAN

1. Purpose:

The purpose of this plan is to identify data needed to define the environment of ambient electromagnetic fields and spectra that are incident upon an aircraft radar surveillance platform with a phased array antenna which uses T/R modules in its active aperture.

2. Definitions:

"electromagnetic environment" - spectral, spatial and temporal distributions of electromagnetic energy or power in which a given system, equipment, device, circuit or component must operate while performing its specified, "designed-for" function.

"spectral, spatial and temporal distributions" - empirical data or the analytical algorithms for generating such data that provide electromagnetic energy profiles in terms of field attributes at given coordinates and locations above the earth, and at specified times or durations: these include intensities, phases, polarizations, average and/or peak power levels, spectral and/or spatial power densities, RF carrier and harmonic frequencies, etc.

"platform" - a description of an emitting and/or receiving structure, vehicle or configuration that includes the geometrical, electrical, physical, avionics and other databases needed to analytically identify and characterize the entry ports of electromagnetic energy.

"electromagnetic environmental effects (E3)" - spectral and temporal responses of a system, equipment, device, circuit or component that are caused by the electromagnetic environment and that degrade, compromise, prevent or otherwise alter the victim's "design-to" performance in its intended environment: the effects may be temporary or permanent.

"E3 drivers" - Thevenin and Norton circuit models that characterize the electromagnetic environmental fields and spectra on the victim platform as equivalent, dependent voltage and current sources that provide ambient environmental energy and power signals to the susceptible ports of entry.

"category I effects" - responses that could result in the loss of life, loss of the platform, a "costly" abort (in the Gigabucks range) or an unacceptable reduction (or loss) of functional performance that <u>will</u> jeopardize the system effectiveness.

"category II effects" - responses that could result in injury, damage to the platform or a reduced functional performance that may jeopardize the system effectiveness.

"category III effects" - responses that could result in annoyance, discomfort or a reduced functional performance that may not jeopardize the system performance.

"category IV effects" - responses that could enable the compromise of classified and/or proprietary data, or the characteristics of the systems and equipment that transmit, receive, store, process, display, print or otherwise handle such data.

"category V effects" - responses that could enable the unauthorized access, manipulation or theft of financial assets, or the characteristics of the systems and equipment that transmit, receive, store, process, display, print or otherwise handle such assets.

3. Data Sources: Candidate sources for a first cut at these data are suggested as:

1) ECAC in Annapolis, MD
2) ROME LAB/IRAE
3) ROME LAB/EE

4. Data Restrictions: Unclassified data are preferred.

5. Data Formats: Data should be format compatible with Rome Lab GEMACS fields type analysis tools.

6. Frequency Range: 100 MHz to 50 GHz.

7. Bandwidth Range: Spectral bandwidths of the power, energy or fields' distributions as available in % bandwidth or as a centered frequency range.

8. Altitude Range: 20 kFt to 60 kFt.

9. Type Fields: whatever fields data are available: i.e., electric, magnetic or both.

10. Intensity Levels: whatever field intensities are available: i.e., dBuv/m.

11. Power Levels: whatever power levels are available: i.e., dBm or dBm/cm2.

12. Polarization: horizontal, vertical, circular, elliptic, random or otherwise.

13. Modulation: modulation characteristics, if available (i.e., CW, AM, FM, PCM, PN, PM, percent modulation, etc.)

14. Type Sources: types of sources generating the environment, if known (i.e., commercial radio and TV, military radar, amateur, etc.)

15. Precipitation Static Levels: average and peak lightning activity in the locale as field levels, if available.

16. Locations: Geographical locations suggested are; 1) Mideast, 2) Northern Europe, 3) Former USSR Republics, 4) Former Yugoslavia Republics, 5) Central Europe, 6) Southwest Asia, 7) Far East, 8) Central America, 9) Northeast Asia

17. Areas: Areas of interest within a global location are:

1) urban
2) rural

18. Temporal Variations: The time variations in the data are of interest, if available:

1) seasonal: i.e., four seasons, averaged over 3 months.
2) weekly: i.e., average of any seven consecutive days.
3) daily: averages of 24 hour periods.

19. Topographies: Natural topographies of interest, if available, are:

1) flat, treeless
2) flat, treed
3) hilly
4) mountainous
5) sandy
6) gullied
7) canyoned
8) marshy
9) deltas
10) salt water
11) fresh water

20. Other:

Any other descriptions of the natural environment and its electromagnetic sources that can in any way relate with the electromagnetic characterization of a vehicle or platform immersed in such an environment.

21. NOTES:

DESIGN AREAS IN T/R MODULES OF CONCERN DUE TO E3 IN MMICs

Background

T/R modules in phased arrays of advanced design, active aperture radars must be robust to operate and survive in wideband, spectrally dense (E3) signal environments. Intrusive coupling from high power, exterior sources, friendly and otherwise, cause upset, distortion and damage in the digital ICs and linear MMICs of a victim module.

Additionally, parasitic coupling of unintended internal sources that interact with a modules' nonlinear circuits, outside of its design bands, produce degrading mix products in-band. The sum result is a synergism of E3 effects and a decreased effectiveness of the array and its host radar. We list below some design areas of concern for T/R module and MMIC environmental interactions.

E3 Design Caveats

1. T/R module and MMIC packaging effects from parasitics and internal field resonances must be avoided.
2. Control stray mutual coupling impedances between radiator elements for stable patterns.
3. Seek internal trace and ground plane layouts for minimal coupling.
4. High speed digital clocks are sources of spurious emissions: avoid where possible.
5. High dynamic range increases IMOD and XMOD susceptibility.
6. Analog signal processing demands minimal distortion in the desired signals' spectra.
7. Common mode grounding among MMIC devices, hybrids, digital circuits and striplines must be avoided.
8. ESD protection networks for MMIC GaAsFETs are susceptible to E3 even when quiescent in the untriggered mode.
9. Short run lengths to minimize stray inductive coupling and radiation are a must.
10. RF bypass capacitors, vias and other interconnects must be linear.
11. Find component layout strategies for a minimal E3 topology.

12. High speed, high density clock lines are sources and sinks of radiation emission and susceptibility.

13. Digital offset, latchup and ground bounce all effect the antenna pattern integrity.

14. Signal harmonics and intermodulation products into any MMIC port can cause distortion and upset.

15. Trace and stripline geometries must be gradual to minimize any emission or coupling at sharp bends.

16. Imbedding ports for MMIC self-test adds circuits which may be more susceptible to the E3 than the baseline MMIC host.

Note: some of these concerns may overlap; some may be the domain of functional designers -- they are included for completeness.

Historical Concerns

During a recent T/R module development program, it was reported that early prototype designs were deficient. Internal parasitic effects at microwave frequencies contributed to the Q of the resonant cavity formed within the module itself. The cavity was driven by RF leakage from the transmitter channel into the receiver causing unacceptable module performance. The design fix added ferrite absorbers into the transmitter cavity to despoil its high Q. The fix worked but added more components to the module with attendant cost penalties.

In designing phased array antennas, one attempts to locate elements close enough to each other in order to synthesize the static pattern without contending with the mutual coupling effects which tend to break up the pattern. The design rules for the radiator separation are usually based on the operating wavelengths. These criteria are "in-band".

However, the input impedances of modules can go nonlinear if subjected to high enough input power levels from any nearby transmitting elements in the environment, or from any other RF sources which may be also on the same platform. The latent nonlinearities in FET's, circulators and diode switchs can contribute unintended mix products, in-band and out-of-band, which cause unacceptable distortion in the desired signals.

A module designer likes to keep his circuit layouts very compact in order to reduce the volume and weight overhead, to reduce the thermal paths to the heat sinks and to minimize the stray, internal coupling. This consideration is usually in-band and the (design-to) trace separations are usually based on those wavelengths for the unwary designer. Unfortunately, this design strategy does not account for the circuit nonlinearities which can produce strong coupling at many unsuspected frequencies.

In addition, coupling caused by radiation from the traces onto the DC rails with only nanohenries of inductance, causes common mode noise to build up in the power conditioner, possibly degrading the noise margins in the digital controller circuits. Upsetting the phase shifter bits degrades the antenna pattern.

Emission levels from clocks and LO's can also couple onto the traces and transmission lines, and be conducted into susceptible FET's and logic IC's. Ground bounce is another problem in the digital circuits of these modules.

Ground bounce occurs when a voltage builds up on a trace inductance. These voltages arise from fast current switching transients at the gates which cause the gate "low" state to seek one of two (or more) ambiguous grounds i.e., the digital chip or the external ground plane. This ground hunting causes degraded BER, enhanced emissions, circuit ringing, and other circuit stresses.

SUMMARY AND RECOMMENDATIONS

Task (1): Vector Modeling of Multi-ports

The concept of a multi-port, vector susceptibility for characterizing E3 in MMICs is shown to be potentially a very useful CAD tool. The time domain matrix formulation presented for modeling memory-less circuits illustrates the scope and utility of a difficult theoretical problem. While its solution vectors could not be completely formulated nor its corresponding frequency domain formulations be found, heuristic memory-less models developed did demonstrate the utility of the relevant multi-port concepts. Analytical difficulties in developing the spectral approach to E3 vector modeling of multi-port MMICs with memory were beyond the resources of this effort.

This initiative should be further pursued with university level, engineering investigations into the nonlinear, multi-port analytics required for vector modeling. These should include time and frequency domain characterizations of the both baseline and E3 performances. The resulting analytical descriptions may be used to develop analysis algorithms suitable for designing a multi-port circuit, vector susceptibility simulator capable of MMIC CAD with a special E3 emphasis.

Task (2): Modeling Assistance

To enhance the E3 modeling capabilities of Rome Laboratory, this task reviewed the current technologies of MCM (multi-chip module) and T/R module packaging. The emphasis of these reviews was to determine any potential impact of E3. In both of these module technologies, the attendant densities of active components and high frequency interconnects strongly suggest potential sources of E3 susceptibility problems.

Visits to industrial based laboratories doing MMIC CAD (for these modules) indicated that while design data are freely open to some extent, their proprietary design data are not normally available. This can be a problem to the E3 oriented customer who attempts to simulate and validate their baseline product designs before doing any E3 related analyses.

It is recommended that government suppliers of MMIC CAD be required to provide or to (at least) allow use of their baseline circuit simulation data so that the MMIC performance can be replicated on government CAD platforms. Even though each case is probably a little different, appropriately tailored contract agreements are needed. These initiatives should be mandated to obtain or have access to the necessary circuit modeling data in order to replicate the baseline MMIC performances whenever E3 simulations are considered. Ownership of these CAD data for the baseline modeling may still be an issue in some cases.

MMIC modeling assistance, in general, can also be enhanced and accelerated by Rome Lab initiatives to exploit the current technology transfer programs. It is recommended these may take the forms of organizing appropriate E3 conferences, workshops, sessions, short courses, or expert discussion panels at local and national levels. Certainly, E3 papers on MMICs and modules by Rome Lab and its contractors are always viable, useful, and very effective means to technology transfer.

To enhance continuity of financial support, it is also recommended that "proofs-of-concept" demonstrations of the E3 susceptibility of MCM and T/R modules be conducted for higher levels of management, especially those with control of the budgets. Showing and demonstrating the degraded performances attendant with E3 in MMICs and modules, provides possible leveraging advocacy to sustain the cause of E3 awareness. These demos can become very compelling arguments to obtain adequate funding for continued E3 technology work in a times of shrinking budgets.

Task (3): Vector Modeling Validation

The time domain, vector susceptibility models developed for this effort are heuristic and confined to memory-less, resistive multi-ports. Limited computer simulations were performed to verify them as multi-ports using industry and Rome Lab data. An LNA and a power amplifier from a Rome Lab T/R module in the 1-10 GHz range were used as first cut, baselines with good results.

Both used Rome Lab FET models which were custom amalgams of available (FET device) parametric data. While the baseline performances compared favorably, measured E3 data were not available to compare with simulations. That the above baselines tracked well is indicative of Rome Lab ingenuity in synthesizing good FET device models from the available data.

Another significant result from this task is the imperative for having good measured data to model the CAD baselines. The circuit parameters of the active FET devices and many of the other microwave circuits must be measured "in situ" for most of the MMICs of E3 interest. These device parametric data are unquestionably essential to accurately simulating the active FET devices used in circuit models. Availability of those data is often denied by proprietary constraints. An alternative may be a robust in-house measurements program for parameter extraction.

Additional validation work is recommended. The purpose is to confirm or validate the vector susceptibility concepts in the other MMIC ports and in the rest of the MMIC suite of the T/R module. These will need more measured data -- parametric data for the device modeling and performance data for comparing both the baseline and E3 with simulations. This initiative could be very productive adjunct to the Task (1) recommendations above.

Task (4): Design Plans

The design plans completed contain approaches to computer-aided modeling and simulation with particular emphasis on the related measurements of MMICs, modules, and the electromagnetic environments of their host platforms. In addition, these plans together with Appendix "A" contain preliminary approaches to modeling and measuring E3 susceptibilities of the newly emerging packaging technologies for MCM (multi-chip modules).

Design plans included herein are: "Some Circuit Parameters Required for the CAD Modeling and Analysis of E3 in MMICs", "Defining an Electromagnetic Environment for Predicting a T/R Module Susceptibility", and "Design Areas in T/R modules of Concern to E3 in MMICs".

To obtain the necessary data to further validate the vector susceptibility concepts developed so far, and to demonstrate the E3 performance degradation in both MMICs and T/R modules, it is recommended that related susceptibility test plans be prepared. These should include plans for conducted and radiated effects' testing using the Rome Lab experimental test facilities.

In addition, there is a need to investigate the possible E3 related issues attendant with integrated test diagnostics. Of special interest are those degrading susceptibility effects which may be unintentionally caused by those imbedded, test dedicated circuits which are provided for the built-in, self-testing of the host circuits.

As a reasonable extension of the present T/R module work, it is recommended that susceptibility modeling and measurements of E3 in advanced packaged MCMs be initiated. These initiatives should include both conducted and radiated effects in the victim MCMs as well as in their constituent circuits. Many of these circuits are functionally digital and may also include other imbedded circuits dedicated for BIST.

While heat dissipation may be a problem in some MMICs, it is always a major design factor in MCMs. It is recommended that a study be performed to determine ways to integrate thermal and electrical design (CAD) techniques into a single CAD program or methodology for doing E3 analyses and assessments of MCMs.

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APPENDIX A

INTEGRATION OF DIAGNOSTIC TECHNOLOGIES

July 10, 1992

Mr. Carmen J. Luvera, Chief
Electromagnetic Systems Division
Rome Laboratory
525 Brooks Road
Griffiss, AFB NY 13441-4505

Dear Mr. Luvera:

Two weeks ago the Electromagnetics and Reliability Directorate of the Rome Laboratory sponsored a three day workshop the Integration of Diagnostic (ID) Technologies.

As you recall, you suggested that my attendance at that workshop would be beneficial to our current work in ERPT on modeling E3 susceptibility of circuits and modules. Your foresight was correct.

The ID workshop turned out to be very enlightening and equally stimulating. From perspectives of E3 modeling and measurements, I noted several areas and opportunities that may be of interest to you.

In the attached report, I am pleased to share these perspectives with you and your associates in the Electromagnetic Systems Division.

Sincerely,

DANIEL J. KENNEALLY
Independent Consultant
Calspan Inc./U.B. Research Center

copy to Rome Laboratory: J. C. Cleary, ERPT
T. W. Blocher, ERPT
M. F. Seifert, ERPT

copy to CUBRC: R. Daley
M. Elardo

INTEGRATION OF DIAGNOSTIC TECHNOLOGIES WORKSHOP

June 23-25, 1992

Mohawk Glen Club
Bldg. 890
Griffiss AFB, NY 13441-5000
(315) 330-7034

Sponsored by:

The Electromagnetics and Reliability Directorate
Rome Laboratory
Griffiss AFB, NY

INTEGRATION OF DIAGNOSTIC TECHNOLOGIES WORKSHOP

MOHAWK GLEN CLUB • JUNE 23-25, 1992 • GRIFFISS AFB, NY

PROGRAM AGENDA

TUESDAY, 23 JUNE 1992

0730 - 0830	Workshop Check-In and Refreshments
0745 - 0820	Speaker's Breakfast for Speakers and Session Chairs Mohawk/Chiefs Room
0830 - 1000	OPENING SESSION Rome Room
	Introductory Remarks 1Lt Antonette S. Pettinato, Rome Laboratory Program Chair
	Welcome Mr. John Bart, Chief Scientist, Reliability Sciences
	Keynote Address Mr. Raymond Hutter Air Force Material Command (I)
1000 - 1015	Coffee Break - Lobby

PLENARY SESSION I

1015 - 1215	Diagnostic Opportunities Paul Abendroth, Aeronautical Systems Division, WPAFB (Chair)
	"Digital Electronics" Don Sterba, Texas Instruments
	"Analog Electronics" Fred Liguori, Naval Air Weapon Center

"Test Buses"
Pat McHugh, Army LABCOM

"Electromagnetic Effects Integrated Diagnostic Capabilities"
Anthony Pesta, Rome Laboratory

Question and Answer Period

1215 - 1315	Lunch - Main Ballroom

PLENARY SESSION II

1315 - 1330	Colonel John M. Borky, Rome Laboratory Commander
1330 - 1515	Diagnostic Integrations Frank Born, Rome Laboratory (Chair)

"Integrating Diagnostics Into Today's Technologies"
R.H. Clothier, General Dynamics

"IDSS Tool Capabilities"
William Keiner, Naval Surface Warfare Center

"Tool Frameworks"
Mike Granieri, Giordano Automation, Inc.

"Applications of the Test Bus"
Wayne Daniel, Texas Instruments

Question and Answer Period

1515 - 1530	Break - Lobby

PLENARY SESSION III

1530 - 1630	The User Perspective - Panel Warren Debany, Rome Laboratory (Chair)

Panel Members:

"Operational Viewpoint"
Capt Ronald Rosenberger, Operational Support Squadron

"Intermediate Maintenance Viewpoint"
Rick Schabener, 416ILMS/LGAME

"Environmental Implications and Diagnostics"
Leonard Popyack, Rome Laboratory

Question and Answer Period

WEDNESDAY, 24 JUNE 1992

PARALLEL WORKING SESSIONS

(A) DESIGN/DEVELOPMENT TOOL TRACK - These sessions will focus on developing a plan/structure for integrating existing diagnostic design/development tools and an ideal plan (near term) for automation of the entire diagnostic specification/design/development capability.

0800 - 1200	WORKING SESSION 1A - Rome Room Design Development Tools - Present Capabilities
0800 - 0815	Eugene Blackburn, Rome Laboratory (Chair) Recorder: Paul Ratazzi
0815 - 0945	2 Minute Presentations Define Issues
0945 - 1000	Break - Lobby
1000 - 1200	Identification of Necessary Elements
1200 - 1300	Lunch - Main Ballroom
1300 - 1700	WORKING SESSION 2A - Rome Room Integration of Design/Development Tools
1300 - 1315	Dr. Warren Debany, Rome Laboratory (Chair) Recorder: 1Lt Antonette S. Pettinato
1315 - 1445	Define Issues
1445 - 1500	Break - Lobby
1500 - 1700	Develop Plan

(B) DIAGNOSTIC TECHNOLOGIES TRACK - These sessions will focus on developing a plan for optimized diagnostic capability using existing technologies and identification of required technologies which are necessary for complete integration of: chip-to-system, on-line to off-line and factory-to-depot diagnostic capability.

0800 - 1200	WORKING SESSION 1B - Liberty Room Diagnostic Technologies
0800 - 0815	Jim Collins, Rome Laboratory (Chair) Recorder: Frank Born
0815 - 0945	2 Minute Presentations Define Issues

0945 - 1000	Break - Lobby
1000 - 1200	Identification of Necessary Elements
1200 - 1300	Lunch - Main Ballroom
1300 - 1700	WORKING SESSION 2B - Liberty Room Integration of Diagnostic Technologies
1300 - 1315	John Bart, Rome Laboratory (Chair) Recorder: Dale Richards
1315 - 1445	Define Issues
1445 - 1500	Break - Lobby
1500 - 1700	Develop Plan

THURSDAY, 25 JUNE 1992

0800 - 1130	PLENARY SESSION IV - WORKING SESSION SYNOPSIS
0800 - 0810	Chair - 1Lt Antonette S. Pettinato Main Ballroom
0810 - 0900	Interchange working groups to evaluate plans A Track - Rome Room B Track - Liberty Room
0900 - 1000	Incorporation of comments by original groups
1000 - 1015	Break
1015 - 1130	Synopsis with entire attendance - Main Ballroom Updates from session chairs of A and B sessions
1130 - 1230	Lunch - On your own
1230 - 1500	Rome Laboratory Tour
1230 - 1310	Electromagnetic System Division (ERP) - Electromagnetic Effects Analysis - Anachoic Chamber
1310 - 1350	Systems Reliability Division (ERS) - Time Stress Measurement Device (TSMD) - Finite Element Analysis/Reliability
1350 - 1430	Microelectronics Reliability Division (ERD) - Reliability Physics/Failure Analysis - Analog Test Facility - Design and Test Automation

INTEGRATION OF DIAGNOSTIC TECHNOLOGIES WORKSHOP

June 23-25, 1992

SUMMARY OBSERVATIONS

Diagnostic test data must be stored on board the platform for subsequent down loading.

Testability and diagnostics must include RF and microwave components of a system.

T/R and multi-chip modules both need buss compatible, test vectors to measure linear and digital performance baselines.

RF test vector sets must contain a priori chosen sub-vectors for critical MMIC tests: first problem is to determine what is performance "critical" in an MMIC RF circuit.

Probes and sensors are needed to implement distributed testability; this is especially relevant to microwave diagnostics.

The TSMD probe needs to measure and record the global and local EM environments in the "vicinity" of an aging part, over real time.

To implement RF DFT test cells in micron scaled, silicon (for digital circuits) and in gallium arsenide (for RF circuits), we need:

Electric and magnetic fields sensors,
EM detectors and analyzers (frequency and time),
Tunable and programmable EM field sources
Noise sources in all the bands

Integrated diagnostics (ID) needs demonstrative proofs-of-concept.

Test beds and beta sites are needed for ID demos at all levels.

All aircraft systems have dynamic surfaces that must be incorporated into any antenna modeling and analysis for system level, EME assessments including the baseline perfromances.

Simulation CAD tools for EME diagnostic analysis at all levels are needed.

EM probes, sensors, and recorders are needed to "snapshot" the part's "immediate" EM environment, especially windowing the time frame in which the part failure or upset occurred.

We need a set of ID definitions consistent among all the players.

Hybrid test vectors are needed for mixed mode test diagnostics.

SPECIFICS

The ER Directorate of the Rome Laboratory recently sponsored a workshop on Integration of Diagnostic Technologies on June 23-25, 1992. The program agenda and list of attendees are attached to this report. Hard copies of the plenary presentations were not made available and would not become available until "some time in late July".

The purpose of the workshop was to review current diagnostic (test) technologies and to formulate plans and approaches in the areas of diagnostic design/development and related technologies. For this, in addition to the plenary sessions, two separate working tracks were convened and devoted to pretty much open forums on (1) design/development tools and (2) diagnostic technologies.

In these workshop forums, each attendee actively participated with their frequent and informal inputs, and a 2 minute presentation on their own needs or requirements for ID (integrated diagnostics). My presentation view graphs on "Electromagnetic Effects in Integrated Diagnostics" are also attached.

After an introduction by the workshop committee chairperson, 1Lt. Antonette S. Pettinato, Mr. Jack Bart of ER gave the welcome address. He outlined some of the goals and the motivation background for such a workshop, and introduced the keynote speaker, Mr. Raymond Hutter of HQ AFMC/ENSP which is the new AF command that combined AFSC and AFLC.

Diagnostic test data must be stored for subsequent down loading to the ground based maintenance levels - O level (flight line), I level (intermediate shop/squadron) and D level (depot level).

Testability and diagnostics are tightly coupled and indispensable attributes of an effective weapon system. Among the goals are reduced vulnerability to down time. For this, effective diagnostic test systems must test, diagnose, and heal in a maintenance cycle of detect, find, and fix any fault. This includes RF and microwave.

One motivation for integrated diagnostics comes from General Yeats' recent directive on ID. On (or about) 28 May he signed a letter articulating a major statement on "Policy on Design to Test". It ordains and requires designs for testability and diagnostics for all Air Force systems with performance verifications based on actual field data.

He is especially interested in correlating the predicted data with the field data using statistical tools that focus on cause and effect; i.e. Pareto charts. This is a new "technical effectiveness" and "design-to-test" policy and is particularly consistent with General Yeats' personnel philosophy of measurements, measurements and more measurements.

The most striking and recurring theme of this meeting was the emphasis on digital systems (!), starting with digital ICs, modules, assemblies, subsystems, etc. ad infinituum, ad nauseam. The voices for analog or linear systems were few. While heard as a polite courtesy, their lot did not seem to invoke much interest or to be enthusiastically heeded.

As some 19th century physicist once said about his contemporaries; "we seem to solve the problems that we already know best...and where the solutions are more tractable and symposium elegant". This report will come back to this issue and develop it in detail as we progress.

The current thrust in systems acquisition is on integrated product development (IPD) which apparently is another buzz word for what IEEE calls "concurrent engineering" and others call "TQM". Testing digital systems now involves mixes of card edge test connectors, BIST (see appendix for list of acronyms and definitions), BIT, and SCAN in what has been called (by the bean counters, no doubt) "value roll-up". This refers to the value added to a product as it progresses upward thorough each step of test in the system hierarchy.

At the module level there is a need for buss compatible, test vectors which contain a priori critical IC test vectors. This kind of DFT requires a lot of modeling efforts that use the new synthesis tools coming on line for digital logic functions. Testing the module infrastructure will needs both internal and external SCAN.

To achieve a reasonable degree of tests that cover the entire populations of components, seeming to grow endlessly in density and complexity, the DFT designer must go to distributed testing architectures which capitalize on extensive use of test busses. The VHSIC phase II program apparently was the first in the industry to develop a standard buss interface for high speed testing (of digital circuits, of course).

In this same context, IEEE issued IEEE Std. 1149.5 on "Test and Maintenance Busses" which became almost an industry "de facto" standard for doing good testable back plane wiring. Another step in digital DFT was the advent of SCAN testing for PC edge card fault and find analysis. Currently, the SCAN trends are both downward to the IC level and upward to the module level. While the former trend is progressing with an acceptable degree of vigor, the latter (module level) is not. In either case, DFT for analog test busses and test cells are sorely needed.

Test maintenance (TM) bussing for effective DFT is presently in a state of flux, a mixed bag. Some government experts predict that the DoD will not issue requirements or standards across the board for TM busses while others, notably industry gurus, predict that the DoD will because it's presently required in some acquisitions.

The group consensus seems to be that with the mass volume usage of IC chips, modules and boards in military system acquisitions as well as in commercial product lines, the associated economies of scale (i.e., "more is cheaper") will naturally gravitate the customer requirements to include TM bussing designs. The most likely places will be at board and module levels with the IC level to follow, given the predicted volumes.

If so, this means loads of chips and modules with boundary scan and other test cells designed and imbedded into their silicon and gallium arsenide architectures. And, on a much larger scale, all kinds of test probes and sensors for a distributed testability in a system should also benefit by exploiting the same economies of scale.

Electromagnetic effects' integrated diagnostics again exemplify the lack of systemic analog and linear (as opposed to digital) test diagnostics and implemented at all levels of a system architecture. It is an undisputable fact that the electromagnetic environment contributes drivers to the physics of fault and failure at the component part level.

Knowing the spectral and temporal characteristics of this EM environment provides extra dimensions to the failure data which will help to identify and sort out the interrelated causes and electromagnetic effects' trends in the data.

In this regard, a TSMD measurement probe could be made immensely more useful if it could measure and record a global EM environment of the aging part over real time. This could provide the trouble shooter with an EM signature, a "snap shot" of EM fields' profile in the environment at the time of failure and, at the same time, provide a temporal history of electromagnetic stresses to the maintenance analyst.

For embedded BIST at RF, we will need tunable and programmable electromagnetic sources: we will need electric and magnetic fields sensors, detectors, and frequency (as well as time domain) analyzers; and we need to implement these diagnostic microwave test cells in micron scaled, silicon and gallium arsenide device structures.

Colonel Borky (Rome Lab's Commander) identified or, at least, articulated a NEW (for me, anyway) aspect of leverage, attendant with (solving) the problem of maintainability -- achieving an increased maintainability from an enhanced repairability through DFT translates into a leveraged increase in inventory assets.

This means that with increased operational up-time, we will need fewer spares in the inventory to sustain a given maintenance figure of merit. In addition, the so called "penalty" of ID really adds value to the performance overhead by making the host/benefactor systems more available and more effective.

Another recurring theme throughout the work shop was the imperative need for demonstrative "proofs of concept". Ways must be found that clearly show and unambiguously prove out the advantages and benefits that accrue from integrating (test) diagnostics in systemic design-for-test.

We need demonstrator test beds or beta sites for integrated diagnostics, testability (technology) insertion. The methods of "proof" must be realistic and direct. The value added which is attendant with and leveraged by doing DFT diagnostics must be shown in straight forward, reasonable, and plausible ways. Even study investigations need ways to demonstrate its utility.

The nonelectronic technologies in system acquisition are not being addressed with any comparable vigor as the electronic. The scope of integrated diagnostics correctly includes all the component technologies of the subsystems that make up an entire weapon system. In the case of an aircraft, this includes air frame, engines, hydraulic, electromechanical, optic, control surfaces, electro-optical, electrical power, ordinance, pilot safety, etc..

In fact, it was stated (and restated many, many times) at the workshop that these make up about 70% of a typical aircraft! Existing integrated diagnostics for the nonelectronic subsystems are presently primitive and in dire need of DFT research and development. Much remains to be done in these areas.

Many of our aircraft have moveable structures on the air frame such as control surfaces, wings and rotodomes. These dynamic surfaces change the boresight and radiation patterns of collocated transmit-receive antennas. Some kind of built-in, adaptive test diagnostics could help here to measure the attendant changes and generate the signal necessary for compensation.

Testing scripts include BIT and external depot. The former can be done when the unit-under-test (UUT) powers up or be done periodically at the command of controller. Vertical testing (and its value added attributes) in a mature system flows up and down through system levels of indenture which include wafer, chip, package, MCM module, board, assembly, and subsystem.

DFT should use a "kernel" approach, starting at the smallest (kernel) level and working upward through the system design. Thus, integrated test diagnostics at the line repairable unit (LRU), the line repairable module (LRM), and at the subassembly repair unit (SRU) are absolute requisites.

From an operational point of view, in particular EW, it was noted that most training missions for ECM are done in simulators. This is because it's just not very practical to get FCC permission to turn on the offensive jammer suite in the CONUS, and almost impossible to obtain similar permission in ETO. The operators stated that EM interference is a common problem from own and external emitters; blankers are still used.

Some off-the-record things heard at the informal group sessions on "diagnostic technologies":

costs of imbedding ID design into chips are incurred mainly during R&D and not during production.

impacting a system life cycle of 10 or more years is not meaningful given the uncertainties involved: we don't even budget that way so we must impact he costs of ID right up front during the R&D phases.

if we can embed enough ID, BIT, and BIST technology into wafers, chips and boards then there is even a chance of "doing away with" the ATE associated with manufacturing which is now a huge investment and a high contributor to overall costs.

simulation methodologies for EME diagnostic analyses at chip, package, and board are needed; and the parametric data to support those analyses.

electromagnetic sensors, both distributed and discrete, are needed in conjunction with TSMD's to snapshot the EM environment at the time of failure.

EME are needed at all levels in all environments.

analog circuit/device testing and simulation need drastic improvements in the areas of fault (abrupt and otherwise) generation, detection, and location. There is presently too much emphasis on digital at the expense of analog or linear.

the digital people say much more needs to be done on sneak circuit analysis: the linear analog people already have encountered this problem a long time ago and called it parasitic (coupling) effects. We need to cross fertilize the two circuit communities.

databases to support ID are needed and especially ways and a system mindset to exploit the data made available.

we need more practical demonstrations of diagnostics as opposed to more theoretical prognostics.

we need to set up definitions that have a common accepted meaning by all the communities who contribute to ID. A gross example which came up time and time again was the term "model".

digital circuit people have many, many meanings mostly derived from software usage, whereas EME people have a few meanings mostly derived from EM circuit and fields engineering and physics. In this regard, it became very apparent that even this short report begged for such a dictionary which is attempted in the attached appendix.

contending with failures, faults, or defects in systems has several facets: avoid, detect, isolate, locate, identify, tolerate, classify, record, and correct - these and more are the integral parts of the integrated diagnostics problem. Each one presents a unique set of sub-problems and opportunities when viewed from EME susceptibility.

Prepared and submitted by: Date:

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APPENDIX
A COLLAGE OF ACRONYMS AND DEFINITIONS FOR INTEGRATED TEST DIAGNOSTICS

CUT: Circuit under test.

UUT: Unit under test.

ATE: Automatic test equipment.

Testability: A measure of how easily tests are performed or how cost-effective it is to perform such testing.

Gold Circuit: A reference circuit whose functional goodness has been (somehow) previously established and which is used as the acceptance benchmark of comparative performance testing: the response vectors of a gold circuit are by definition always correct for any input test vector.

Daisy Chain: A shift-register mode of testing in which all the flip-flops of an IC under test are connected together in a serial chain and sequentially shift out arbitrary test patterns inputted and stored in the FFs.

Ad Hoc Design-for-test: Methods and designs for a given particular, local circuit which are generally not applicable to other designs.

Structured Design-for-Test: Generic methods for solving the testability problem for global classes of circuits.

Bus Structured Architecture: A way of logically partitioning the functions of a logic system by interconnecting them with bidirectional paths for common data exchange. Common busses are data, address and control.

Degating Logic: added logic gates to decouple or disconnect one portion of the logic under test from another portion of logic circuit.

Bed-of-Nails Tester: a planar array of spring loaded pins that make pressure contacts with the IC chips (CUTs) pins on the opposite side of the PWB: an array of tester probes for isolating and controlling the input test vectors, and detecting the subsequent test responses in the CUTs.

Controllability: an attribute of testing in which the known initial state of a CUT can be easily set to a desired state consistent with the test to be performed: sets all the initial conditions to some known vectors prior to testing.

SCAN Design: the ability to input and shift arbitrary test bit patterns into and out of sequential circuits and to observe the resulting bit patterns of all the output states.

TM: test maintenance; usually with busses.

BS: a boundary scan implementation for diagnostics in which all the gates of an IC or module under test are interconnected together to form a daisy chain shift register; test controllability and observability are provide by embedding extra gates or test cells near the IC or module pins (hence a "boundary").

Silicon Overhead: a reference to the amount of chip real estate devoted to providing the extra gates or cells for embedded diagnostics: typically, four to five gates per IC pin which for VLSI is about 15-20% of the host chip.

Functional Testing: the methodology and assets needed to determine that a UUT in a given environment actually performs the design baseline that the designer intended.

Diagnostic Testing: a methodology and assets needed to detect, localize, record and correct performance faults or defects as parameter departures from the functional baselines.

BIST: built in self test.

BIT: built in test.

LRU: line repairable unit (and sometimes "least", meaning one level above throw away).

LRM: line repairable module.

SRU: subassembly repair unit.

Culture: a popular buzzword that describes the fact that many of the pragmatic procedures in a given technology (i.e., ways of doing that technology business) are so widely used and accepted as to have become ingrained without any further question into the contemporary mindset.

Vaporware: in the same context of hardware, software or firmware; "vaporware" refers to some kind of "ware" that exists only in the words we use to describe it.

Paradyne: another buzzword used extensively in ID to denote an exceptionally clear or typical example of how similar things compare to each other; also, an original pattern or model representation from which similar copies are made.

Test Verticality: in a given architecture, diagnostic testing which flows on paths that go up or down the system hierarchy.

Prognostic Maintenance: a maintenance methodology in which operating components are selectively replaced based on predictions of their expected failure.

Adaptive Diagnostics: a methodology of diagnostics in which the test strategies for generation, control and observability change and adapt to the test data produced in order to minimize the total test time and cost.

ID: integrated or integrating diagnostics - a term that encompasses all the technologies and other related components which are required to build, field, support and fight a modern weapon system.

Leveraging: another popular buzzword that refers to an multi-fold increase in an attribute or parameter of a system because of a minor change in another: the operational people call it "force multiplier" wherein our smart weapon systems can be counted to "virtually outnumber" a numerically, but dumber (i.e. not equipped with smart weapons), superior force.

Value Added: the incremental increase in the value of a product as it passes through successful levels of test indenture: each additional level of testing adds its own costs of testing to the total value of the unit.

GIMADS: Generic Integrated Maintenance Diagnostics is a multi-contractor, on-going program which attempts to combine innovative design-for-test with integrated logistical support. General Dynamics/Fort Worth is prime.

DFT: Design-for-test.

CND: means a "cannot duplicate" fault condition of a component which fails in service but does not in manual test.

Digital: an attribute of a circuit or module that describes a finite set of discrete time and waveform levels (usually binary) necessary to perform a logic function.

Analog (or Linear): an attribute of a circuit of module that describes a continuum of time and waveform levels necessary to perform its circuit function.

IPD : integrated product development.

Distributed Testing: an approach to embedded testing that puts the testing cells needed for generation, control, observability as close as possible to cover a maximum number of test nodes.

Levels of Indenture: a popular buzzword to indicate that something can be subdivided into smaller pieces which themselves are further divisible, etc.: the indenture context comes from the indenting we do in technical style writing.

Information Authority: an administrative level in a maintenance structure that temporarily has the most test information about a system or product at any given time is the "authority".

MCM: a multi-chip module is made up of insulating tiers of passivated substrates which contain the chip devices; the IC devices in the tiers are interconnected in wiring planes and the tiers are interconnected vertically at the edges.

Value Roll-Up: see Value Added.

EME: Electromagnetic environment is the collective conditions of dynamic and static, electric and magnetic fields that surround and permeate the vicinity of any operating part of any weapon system when itself is surrounded by external electromagnetic fields: common sources for these environments are intended and unintended, friendly and unfriendly emitters of electromagnetic energy.

Stuck-at-Zero or stuck-at-One: a very common fault in sequential digital circuitry in which a wire or pin goes to the correct logic level on command as intended but then remains there when commanded otherwise.

SUT: system under test.

Walking Pattern: a simple test vector made up of an alternating sequence of ones and zeros which are shifting into and out of a boundary scan, shift register: often used in scan testing of the digital ICs in a sequential machine by making the machine under test essentially combinational.

In-Circuit Testing: another way of saying embedded diagnostics in which the each chip on a board is made testably independent from the other ICs that happen to be present on the same board: chips not under test are disabled or are set to some known states (see Degating Logic).

DATE: 24 JUNE 1992

TOPIC: 2 MINUTE PRESENTATION ON "ELECTROMAGNETIC EFFECTS (EME) IN INTEGRATED DIAGNOSTICS"

SPEAKER: DAN KENNEALLY
CALSPAN/UB RESEARCH CENTER, ROME, NY

SYNOPSIS: Embedding BIST and BS test cells in vertical (system) test architectures may make the host levels more susceptible to (performance) degrading EME, i.e., chips, DIPs, MCMs, PWBs, etc.

ELECTROMAGNETIC EFFECTS IN INTEGRATED DIAGNOSTICS

Baseline Concept:

* Embedded BIST and BS test cells presently sense, detect, localize and measure functional + operating fidelity of IC chips, DIPs, MCMs, hybrid modules, PWBs, sub assemblies, et al.

Design Guides:

* IEEE Std 1149.1 - TAP and BS Architecture
  Mil-Std 1814 - ID and Roadmap Requirements
  USAF Policy Letter - DFT including RF/Metrics
  IEEE Std 1149.5 - Test Maintenance Busses
  AFGS 87256 - Integrated Diagnostics

ELECTROMAGNETIC EFFECTS CAVEATS

Unwanted, unintended EM energy, both radiated and conducted, cause upset, distortion and failure in EM susceptible, circuit and module victims

Embedded BIST and BS cells may make the host levels of system architecture more susceptible to (performance) degrading EME

ELECTROMAGNETIC EFFECTS ISSUES IN EMBEDDED DIAGNOSTICS

* Characterize in situ implementations - EM modeling and measurements

* Measure and store a snapshot profile of EM environment at times of failures

* Synthesize circuit and module topologies for minimal EM susceptibility

* Incorporate embedded test diagnostics into EM fields and circuits CAD analyses

APPENDIX B

CONTEMPORARY GaAs FET MODELS

A MESFET Model for Use in the Design of GaAs Integrated Circuits

WALTER R. CURTICE, SENIOR MEMBER, IEEE

Abstract—A MESFET model is presented that is suitable for use in conventional, time-domain circuit simulation programs. The parameters of the model are evaluated either from experimental data or from more detailed device analysis. The model is shown to be more complete than earlier models, which neglect transit-time and other effects. An integrated circuit (IC) design example is discussed.

I. Introduction

THE PURPOSE of this paper is to present a reasonably simple analytical model for the GaAs MESFET that is appropriate for use in circuit simulation programs. A number of presently available models will be reviewed and criteria for accurate modeling will be presented. Several examples of logic circuit simulation will be described.

The design and development of GaAs integrated circuits (IC's) is aided considerably if circuits may be studied using high-speed computers. Many large computer programs are available for studying dc and transient characteristics of complex combinations of transistors, resistors, capacitors and inductors. However, the success of the mathematical simulation depends totally on the accuracy of the mathematical model. The model must reflect the exact physical properties of the circuit.

The difficulty with MESFET devices is that they are extremely complex internally and simple external models cannot accurately describe their behavior under all conditions. Conversely, a detailed two-dimensional (internal) model [1]–[4] of the device, although more accurate, is not suitable for use with circuit simulation programs.

One approach is to then develop an external characterization of the particular MESFET devices used in the circuit under study. That is, the model used will not attempt to be complete enough for all ranges of device parameters.

A number of MESFET models can be found in the literature. Madjar and Rosenbaum [5] utilize the two-dimensional model of Yamaguchi and Kodera [3] to produce analytical relationships for drain and gate currents as a function of drain–source voltage, gate–source voltage, and their derivatives. This approach appears useful for studying the interaction between the device with its parasitics and its external circuits, such as in frequency multiplier operation. However, the technique would not

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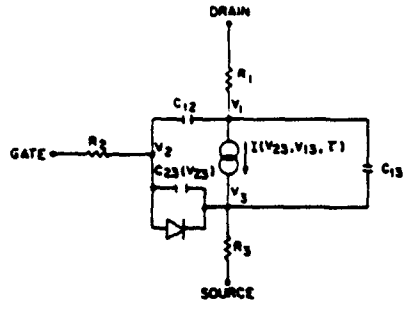

Fig. 1. Circuit model of a GaAs MESFET for use with a circuit analysis program.

be practical in the simulation of circuits with multiple-interacting devices.

Rauscher and Willing [6] have simulated FET amplifiers and oscillators in the time domain with a nonlinear-circuit-type model that includes elements representing the high field domain. Values for the linear and nonlinear elements are determined from *S*-parameter measurements at many bias conditions. The elements with essentially bias-independent values are considered linear. The model has not been applied for circuits with multiple FET's.

A simplified analytical model has been formulated by Shur [7]. He has used Shockley's equations and the assumption that current saturation occurs due to the formation of a stationary Gunn domain at the drain side of the gate when the average electric field under the gate equals the domain sustaining field given as: v_s/μ (v_s is the saturation drift velocity, μ is the low field mobility). The MESFET equivalent circuit is similar to the circuit to be described here; however, electron transit time effects under the gate have been omitted.

The JFET model in SPICE 2 [8] is widely available for circuit simulation studies. However, this model has several deficiencies when applied for GaAs MESFET's. As will be shown, this model is quite in error with regard to drain current–voltage relationships below current saturation. Furthermore, electron transit-time effects under the gate are omitted.

The most complete analytical model is presented by Van Tuyl and Liechti [9]. It is similar to the model to be described here but is slightly more complicated. Computer simulation of a MESFET frequency divider operating at 2 GHz showed excellent agreement with experimental data [10].

Pucel *et al.* [11] present a small signal model and show how to derive the element values. Krumm *et al.* [12] use a similar model but include electron transit-time effects as a time delay factor associated with the drain current source. Good agreement is shown for *S*-parameter data over a broad frequency range (2 to 18 GHz). A MESFET circuit model for transient simulations should not be very different than those models verified for small signal operation in the frequency domain.

Fig. 1 is the proposed large-signal model for the GaAs MESFET. It consists primarily of a voltage-controlled current source $I(V_{23}, V_{13}, \tau)$, three interelectrode capacitors, and a clamping diode between gate and source. Resistors R_1, R_2, and R_3 represent resistance of the contact regions. The only nonlinear elements are $I(V_{23}, V_{13}, \tau)$ and $C_{23}(V_{23})$. The important aspects of the evaluation of these elements will now be described.

II. Properties of an Accurate MESFET Model

The properties that an MESFET model must contain for accurate transient simulation will now be reviewed.

A. Accurate Approximation to the Drain Current Control Characteristics

The drain current relationship to drain–source voltage and gate–source voltage is usually known either from experimental measurements of test devices or from detailed device calculations. The MESFET model must use analytical expressions to approximate this relationship. Often several parameters are required and must be determined by curve fitting techniques. Analytical analysis of the symmetrical JFET model (see Sze [13]) results in a (gate) voltage-controlled drain current source (in the current saturation region) of the form

$$I_{DS} = I_p\left[1 + \frac{V_{GS} + V_{BI}}{V_p}\right]^N \tag{1}$$

where I_p is the "pinch off current" as defined by Sze and more commonly called saturation current, V_p is the pinch off voltage which is $qN_0a^2/(2\epsilon)$ for uniform doping, V_{BI} is the built in voltage at the gate (a negative voltage), V_{GS} is the gate–source voltage, a is the active layer thickness, and N_0 is the donor value. N is found to vary between 2.0 and 2.25, depending upon the charge distribution assumed. It will be seen that the square-law assumption is quite good for real devices.

A second form of control characteristic assumed by Fair [14] and others is

$$I_{DS} = I_p\left[1 - \sqrt{\frac{|V_{GS} + V_{BI}|}{V_p}}\right]. \tag{2}$$

This equation is also used only in the region of current saturation. This form is obtained by assuming that the depletion thickness is the same as that obtained in an abrupt junction, or

$$\sqrt{\frac{|V_{GS} + V_{BI}| \cdot 2a}{q \cdot N}}. \tag{3}$$

The current is proportional to the conduction channel width which is "a" less expression (3). By using the definition of pinchoff voltage V_p, equation (2) can be derived for the case of uniform doping.

Equations (1) and (2) may appear to be quite different; however, in most cases, either one may be used to describe experimental devices. This can be seen by the following illustration. Assume a MESFET exactly follows (2). Fig. 2 is a graph of $\sqrt{I_{DS}/I_p}$ as a function of $(V_{GS} + V_{BI})/V_p$. Notice that it is nearly a linear function between

ordinate values of 0.1 and 0.9. Fig. 2 shows a straight line approximation, which has the equation

$$I_{DS} = 0.8\, I_p \left[1 + \frac{V_{GS} + V_{BI}}{1.25\, V_p} \right]^2. \tag{4}$$

This straight line approximation results in less than 2 percent (of I_p) error in the evaluation of current for ordinate values between 0.1 and 0.9. Equation (4) is just equation (1) with $N=2$ and I_p and V_p multiplied by constants. These constants have no physical significance since I_p and V_p would be determined from experimental data for $I_{DS}(V_{GS})$.

The must serious difference between the straight line approximation and (2) occurs near pinchoff, where current is quite small. Usually, this introduces little error.

Equation (1) can be put in a standard form as

$$I_{DS} = \beta (V_{GS} + V_T)^2 \tag{5}$$

where V_T is the threshold voltage measured from gate to source $V_T = V_p + V_{BI}$, and $\beta = I_p / V_p^2$.

Equation (5) is the form used in the general circuit analysis program SPICE 2. β and V_T are determined by plotting $\sqrt{I_{DS}}$ versus V_{GS}. If actual experimental values of I_{DS} are used, then a current source without source resistance is being described. To develop the model of Fig. 1, the raw data must first be processed to remove the effects of R_1 and R_3. This can easily be accomplished once the values of R_1 and R_3 are determined either by measurements [15] or by calculations. Since the voltage drop across R_3 is typically not negligible, the presence of R_3 usually has a major effect.

The current saturation in GaAs MESFET's occurs at lower voltages than in silicon devices because of the much larger low field mobility. This results in a much stronger current saturation effect. Van Tuyl and Liechti [9] point out that the hyperbolic tangent function provides a good analytical expression for current saturation in GaAs. In addition, one also wants to be able to describe drain–source conductance effects. This is not adequately described by adding a shunt resistor across $I(V_{23}, V_{13}, \tau)$ because current pinchoff is lost. The expression used in SPICE 2 seems to fit experimental devices quite well in the region of current saturation. However the fit is quite poor below current saturation. The expressions used in SPICE 2 are derived from the FET model of Shichman and Hodges [15] and are (for $V_{13} > 0$)

$$I(V_{23}, V_{13}) = \begin{cases} 0, & V_{23} + V_T < 0 \\ \beta (V_{23} + V_T)^2 (1 + \lambda V_{13}), & 0 < V_{23} + V_T < V_{13} \\ \beta V_{13} [2(V_{23} + V_T) - V_{13}] (1 + \lambda V_{13}), & 0 < V_{13} < V_{23} + V_T \end{cases} \tag{6}$$

where

$$V_{23} = V_2 - V_3$$
$$V_{13} = V_1 - V_3$$

and β and λ are constants.

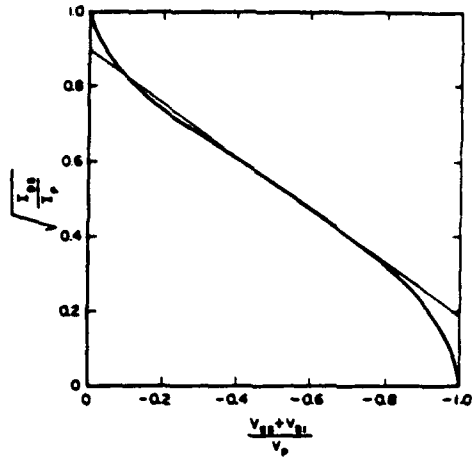

Fig. 2. Value of $\sqrt{I_{DS}/I_p}$ as a function of gate–source voltage for FET devices obeying (2).

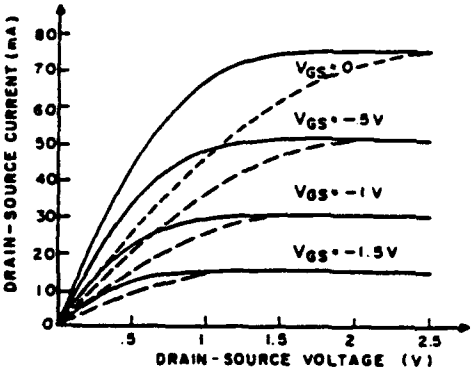

Fig. 3. Best-fit approximation to experimental MESFET I–V characteristics of [8] using the current source described by (7)—(solid lines) and by the JFET model of SPICE 2—(dashed lines). Constants are $R_1 = R_3 = 3\ \Omega$, $\alpha = 2.3\ V^{-1}$, $\beta = 13.1$ mA, $V_T = 2.63$ V, $\lambda = 0$.

The use of the hyperbolic tangent function greatly improves the usefulness of the equation below saturation. The following analytical function is proposed for description of the current source in GaAs MESFET's:

$$I(V_{23}, V_{13}) = \beta (V_{23} + V_T)^2 \cdot (1 + \lambda V_{13}) \tanh \alpha V_{13} \tag{7}$$

where α and λ are constants. Notice that there are four parameters to be evaluated in this expression.

Equation (7) was used to approximate a set of measured drain current–voltage relationships presented by Van Tuyl and Liechti [9]. The experimental data can be matched quite accurately. Fig. 3 shows the characteristics calculated from (7). For comparison purpose, the JFET model of SPICE 2 (6) was also used and these computations are shown in Fig. 3 as dashed lines. Notice that although the gate control is accurately given by both models in the region of current saturation, the SPICE 2 calculations are quite in error below current saturation due to the lack of a parameter to adjust the saturation point. This is a major deficiency of the SPICE 2 model and leads to significant error in computations of switching characteristics.

Equation (7) was also used to approximate the experimental data presented by Pucel *et al.* [11] for a 1-μm MESFET with current voltage characteristics quite different than the previous case. Fig. 4 shows the drain–source characteristic calculated from the model with the parameters listed and the experimental points are also indicated. It is seen that this simple model with analytic current expression provides a good approximation to the experimental device's current–voltage characteristic.

B. Inclusion of Transit-Time Effects

During transient operation, a change in gate voltage does not cause an instantaneous change in drain–source conduction current. This results because in order for conduction current to change, the electron depletion width under the gate must be changed and this occurs by charge transport at a maximum velocity of 1×10^7 cm/s. Thus, it takes of the order of 10 ps for a change in current after the gate voltage is changed in a 1-μm gate length MESFET. (Notice that in the physical device, this charge change is part of the gate capacitance change whereas in the model, we have separated the capacitance and current effects.) The most important result of this effect is a time delay produced between gate–source voltage and drain current. Therefore, the current source (7)

$$I[V_{23}(t), V_{13}]$$

should be altered to be

$$I[V_{23}(t-\tau), V_{13}]$$

where τ is equal to the transit time under the gate.

The time delay effect is not easily added to most circuit analysis programs. We have found a technique that accurately approximates the effect but is simple to calculate. The current source is assumed to be of the form

$$I(V)-\tau\frac{dI(V)}{dt} \tag{8}$$

where the derivative is evaluated as

$$\frac{dI(V)}{dt}=\left[\frac{\partial I(V)}{\partial V_{23}}\right]_{V_{13}}\cdot\frac{dV_{23}}{dt}. \tag{9}$$

The second term in expression (8) is a correction term which may be thought of as the first term of the expansion of $I(t-\tau)$ in time. An error is generated when the gate-to-source voltage has a nonzero second derivative. However, for small values of τ, the error is quite small. In addition, the gate's capacitance helps smooth voltage changes.

Fig. 5 shows the drain current calculated for a 1-μm MESFET device with constant drain–source voltage (3 V) and a gate voltage change from −0.5 V to +0.5 V in 100 ps. The current delay seen for the case of $\tau=0$ is produced by the time involved in charging the gate capacitance. The current delay seen for the case of $\tau=10$ ps is the total delay through the device. Here it is seen that there is some compromise at the beginning and end of the output current waveform but the majority of the waveform is properly time shifted by 10 ps. Fig. 5 shows that if τ is not included at all; then an important source of delay in any MESFET circuit is omitted.

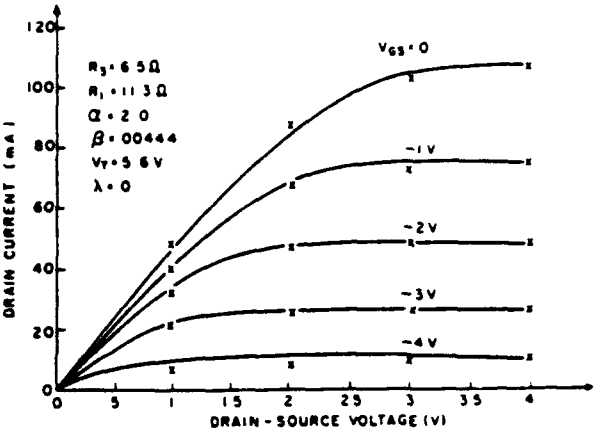

Fig. 4. Best-fit approximation to experimental MESFET I–V characteristics (X) of [10] using the current source described by (7)—(solid lines).

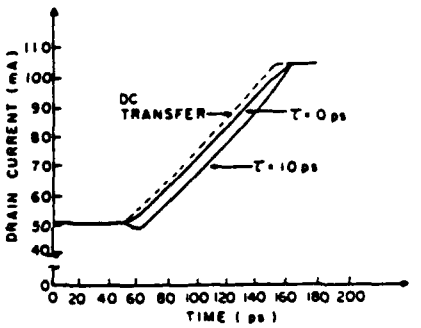

Fig. 5. Calculated drain current as a function of time for a 1-μm gate length MESFET (500-μm width) for a gate-voltage change from −0.5 to +0.5 V in 100 ps with delay time τ as parameter and $V_{DS}=3.0$ V. Constants are same as in Fig. 3 and $C_{23}(0)=0.5$ pF, $C_{12}=0.03$ pF, $C_{13}=0.1$ pF, $V_{bi}=1.0$ V, $R_2=10\,\Omega$.

There will also be some transit-time effect produced by drain–source voltage changes if there is a corresponding change in drain–source current. This effect should only be significant for drain–source voltages below current saturation and is not presently accounted for in this model.

The proposed model includes transit-time effects in driving transistors and in source-follower transistors but not in transistors used for active loads since $dV_{23}/dt=0$. A MESFET logic circuit would use all three types of operation (see Van Tuyl and Liechti [9]).

C. Accurate Evaluation of Gate Capacitance

The charge depletion region beneath the gate produces gate capacitance between the gate and the source C_{23} and between the gate and the drain C_{12}. Each capacitor may be thought of as a Schottky-barrier diode with voltage dependent capacitance. For a negative gate–source voltage and small drain–source voltage, each diode is back biased about the same amount and the capacitances C_{12}

and C_{23} are about equal. However, as the drain–source voltage is increased, more depletion exists on the drain side of the gate compared to the source side and C_{12} becomes smaller than C_{23}. When drain–source voltage is increased beyond the point of current saturation, C_{12} is much more heavily back-biased than C_{23}, and the charge depletion region even extends well out from the gate toward the drain. In the case $C_{12} \ll C_{23}$. These observation have been made by study of the results of the two-dimensional simulation of MESFET's.

Since the voltage drop between the source and the conductive region beneath the gate is always small, the gate–source capacitance C_{23} is usually significant and dominates the input impedance of the MESFET. For many MESFET devices, this capacitance varies much like a simple Schottky-barrier diode capacitance. This capacitance can be easily measured as a function of gate bias with or without drain–source bias. In the model of Fig. 1, drain–source bias should be used while capacitance is being measured. The voltage V_{23} must be determined from V_{GS} knowing R_3.

An analytical expression of the form derived for an ideal metal–semiconductor junction (17) is usually able to approximate such data; such as

$$C_{23}(V_{23}) = \frac{C_{23}(0)}{\sqrt{1 - V_{23}/V_{BI}}} \tag{10}$$

where V_{BI} is the built in voltage. However, the denominator must not be allowed to approach zero as V_{23} approaches V_{BI}. The capacitance will increase as the depletion width reduces and as a forward bias condition occurs, diffusion capacitance will become important. Approximation of this condition may be important for enhancement-type MESFET's.

The built in voltage V_{BI} should be evaluated experimentally from capacitance data. It should be equal to the built-in voltage of the Schottky-barrier junction pulse some part of the voltage drop along the conducing channel under the gate.

It is interesting that (10) which is derived from a two-terminal model is a good approximation for the three-terminal MESFET. The reason seems to be that the gate–source capacitance is a very weak function of drain–source voltage, once current saturation has occurred (in MESFET's not exhibiting domain effects). As the drain voltage is increased (above the voltage of current saturation) the voltage in the conducting channel beneath the gate changes little and there is an increased voltage drop across the conducting region between the gate and drain.

A two-dimensional transient simulation of a typical 1-μm gate length MESFET was used to study the gate–source and gate–drain capacitance due to internal space charge. This analysis is quite similar to that presented by Yamaguchi *et al.* [3] and Wada and Frey [4] and is an extension of the two-dimensional modeling technique described by Curtice [18]. Both C_{13} and C_{23} can

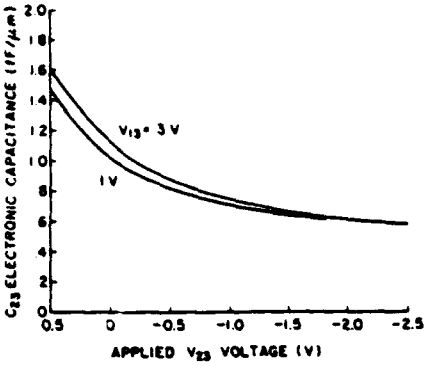

Fig. 6. Electronic gate–source capacitance as a function of gate–source voltage V_{23} and drain–source voltage V_{13} calculated from the two-dimensional model for a 1-μm GaAs MESFET with donor density = $7 \times 10^{16}/cm^3$ and epilayer thickness = 0.25 μm.

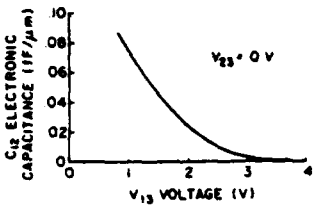

Fig. 7. Electronic drain–gate capacitance as a function of drain–source voltage V_{13} calculated from the two-dimensional model for a 1-μm GaAs MESFET with donor density = $7 \times 10^{16}/cm^3$ and epilayer thickness = 0.25 μm.

be studied for a given device structure using the two dimensional simulation. Some results are presented in Figs. 6 and 7 for a uniformly doped device of $a = 0.25$ μm and donor density = $7 \times 10^{16}/cm^3$ Field-dependent diffusion is included and V_{BI} is taken to be 0.5 V.

The gate–source capacitance is evaluated from the total change flow due to gate displacement current produced by a charge in gate-to-source voltage. Gate–drain capacitance is found from gate displacement produced by a change in drain–source voltage.

Fig. 6 shows that there is little change in the gate–source capacitance as a function of internal drain–source voltage V_{13} above current saturation. But observe that the voltage drop across R_3 may cause a change in gate–source capacitance as the external drain–source voltage is changed if there is significant change in drain current (due to finite drain resistance).

Fig. 6 also shows good agreement with (10). However, the value of V_{BI} that must be used is that due to the Schottky barrier junction *plus* a contribution of about 0.5 V apparently due to the voltage drop in the conduction channel under the gate.

The calculated values of gate–drain capacitance were quite small but increasing with reduction of drain–source voltage, as shown in Fig. 7. As we shall see in the next section, the electrostatic capacitance between gate and drain will usually be much larger than these values. However, if calculations or measurements show that C_{12} is an important voltage-variable capacitance, then it must be

included in the model. Willing *et al.* [19] present data for such a case. This effect is not related to the Miller effect, which is fully included when simulation is performed with loading on the MESFET.

When the active layer thickness and donor value are large enough, in stationary charge accumulation region can exist beneath the drain edge of the gate and just above the substrate interface. The charge accumulation region together with the charge depletion region adjacent to it on the drain side form the stationary high-field domains reported by Yamaguchi *et al.*, Wada and Frey, and others. For the device studied here, only a small amount of charge accumulation is present and only for the case of near zero gate–source bias voltage. If the domain is present over much of the operating range of the device, the interelectrode capacitances may be affected as well as the current control characteristics. The gate–drain capacitance is increased due to the smaller depletion region and the gate–source capacitance may become a strong function of the drain–source voltage as well as the gate–source voltage. Willing *et al.* [19] show such a case. Such domain effects can be important in power MESFET's but are usually less important in devices used in integrated circuit that are typically of lower donor-thickness product [20].

D. Evaluation of "Nonelectronic" Drain–Gate and Source–Gate Capacitances

Experimental drain–gate and source–gate capacitances depend very little upon the operating biases. They are determined primarily by the electrostatic coupling between parallel conductors, quite independent of the internal space charge distribution. From exact solutions of the simplified theoretical problem, Pucel *et al.* [11] have calculated and plotted the drain–gate and source–gate capacitances as functions of electrode separation. Gate length is a parameter for drain gate capacitance and source (or drain) length is a parameter for source–drain capacitance. The geometry is planar and no ground plane is present. The authors state that the source–drain capacitances are in good agreement with experimental measurements whereas the drain–gate capacitances are somewhat higher than the experimental values. Typical values for gate–drain and drain–source capacitance are thus 0.1 fF/μm and 0.15 fF/ωm, respectively.

E. Evaluation of Circuit Parasitics

As the MESFET circuit is made smaller, the pad capacitances and other parasitics become more important. For example, the capacitance-to-ground of the drain contact of a driver transistor can cause significant loading. The metal line providing signal transmission between logic gates of an IC can also introduce capacitive loading effects to ground and also capacitive coupling (or mutual capacitance) effects to other signal transmission lines.

There are several methods of estimating the fringe capacitive effects of a particular IC layout. Maupin *et al.* [21] have computed the complete capacitance matrix (i.e., interelectrode capacitances and capacitances to ground) for the metal contact pads (source, gate, and drain) of each MESFET type and in their circuit. This computation is done by theoretical analysis assuming a ground plane under the substrate.

A second method is to build scaled-up models of the MESFET circuits and to measure interelectrode capacitance and capacitances to ground. VanTuyl *et al.* [10] define metal layouts 10 times actual size and on sapphire substrates. A standard capacitance bridge is used. Excellent agreement with theoretically computed values of capacitance of simple shapes was found. This technique has enabled them to reduce their propagation delay through reduction of parasitic capacitances with improved layout designs.

A dramatic example of the importance of circuit parasitics is presented by VanTuyl, Liechti *et al.* [10],[22]. They show that for a given circuit layout, the propagation delay of a gate is equal to a constant plus a term inversely proportional to transistor width. These two terms become equal at a (buffer) transistor width somewhat less than 10 μm. At this point, the parasitics have doubled the inherent delay of the gate.

III. Dual-Gate FET Modeling

The dual-gate MESFET structure must also be modeled since it is useful for performing ANDing. Asai *et al.* [23] showed that the dual-gate device behaves similar to two FET's in series with each device somewhat inhibiting the operation of the other.

Fig. 8 shows the equivalent circuit assumed for simulation of the dual-gate device. The two equivalent FET's, designated as FET 1 and FET 2 in the figure, consists of a voltage-controlled current source and a voltage-variable gate capacitance as described in Section II.

The saturation current of the dual-gate device is less than that of a single-gate FET. In addition, the g_m of the second gate is lower than the g_m of the first gate because the second device (FET 2) has the first device (FET 1) as a source resistance.

To help offset these effects, the second gate section of the device is usually made 25 to 50 percent wider than the first gate. Fig. 9 shows how the calculated saturation current of the device changes with the width ratio. This calculation assumes parameters typical of a 1-μm gate length MESFET. The width at FET 1 is 500 μm. In addition to lower current, the dual-gate FET has a higher "knee" voltage, i.e., current saturation occurs at a larger drain–source voltage.

To observe the transient response of the dual-gate device, a logic gate was simulated with two dual-gate FET's in parallel as drivers. This is the equivalent of two 2-input NAND gates feeding an OR gate. A width ratio of 1.5 was used for both FET's and the fanout was assumed to be unity. Table I shows the calculated propagation delays for switching with either gate and for an equivalent single gate driver. The relationship of the numbers is quite similar to the measurements by Van Tuyl *et al.* [10]. This

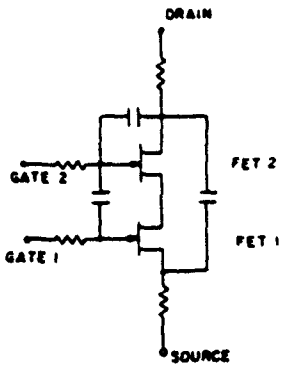

Fig. 8. Equivalent circuit for the dual-gate MESFET.

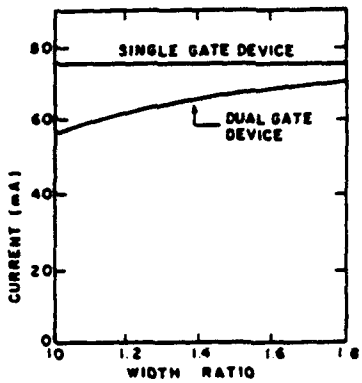

Fig. 9. Saturation current of the dual-gate MESFET as a function of the width ratio at the gates. Constants are same as in Fig. 3 and $V_{GS}=0$.

TABLE I

CALCULATED PROPAGATE DELAYS FOR NAND/NOR GATE

	Propagation Delay (ps)
Using Upper Gate:	80
Using Lower Gate:	87
Using Single Gate FET:	67

is thus good justification for the model. In addition, it is clear that there is a significant increase in the propagation delay for dual-gate devices as compared to single-gate FET's.

IV. SIMULATION EXAMPLE

The model shown in Fig. 1 may be used with a circuit simulation program to study complex integrated circuits. The circuit simulation program used here is R-CAP(24). It is similar to SPICE 2 in many respects but has the advantage that a user-defined device model can be included without difficulty. The model for the GaAs MESFET was added to R-CAP as a subroutine.

The first circuit example is a MESFET amplifier with nonlinear load and is shown in Fig. 10. This circuit is a logic gate without the level-shifting stage. Assuming certain device parameters, the circuit was simulated using R-CAP, SPICE 2 and also by the two-dimensional modeling program. The individual device characteristic were

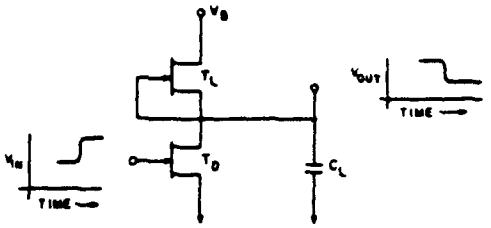

Fig. 10 MESFET logic gate without the level-shifting circuit. MESFET T_L is the same but one-half the width of MESFET T_D.

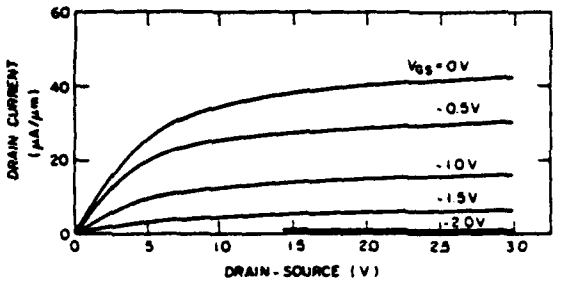

Fig. 11. Drain–source current–voltage relationship for a GaAs MESFET calculated by the two-dimensional program assuming gate length = 1.0 μm, donor value = $3\times10^{16}/cm^3$, active layer thickness = 0.25 μm, built-in voltage = 0.5 V.

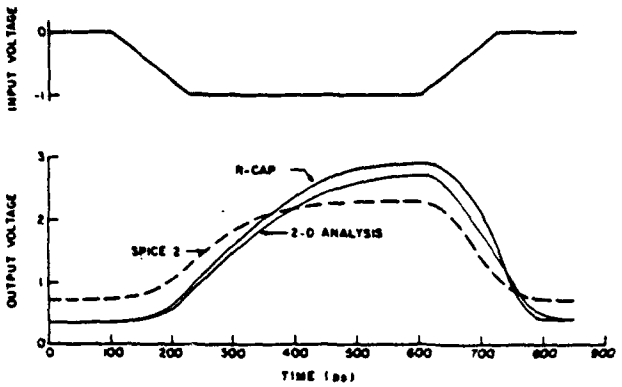

Fig. 12. Comparison of simulation results using R-CAP, SPICE 2 and the two-dimensional analysis for the device of Fig. 11 with $V_B=3.5$ V and for SPICE 2: $V_T=2.5$ V, $\beta=71$ μA/V², $\lambda=0$, $V_{BI}=0.5$ V, $C_{23}(0)=6$ fF, $C_{12}(0)=1$ fF, for R-CAP: $\alpha=1.5/V$, $\beta=65$ μA/V², $V_T=2.5$ V, $V_{BI}=0.5$ V, $C_{23}(0)=6$ fF, $C_{12}=0.3$ fF, $\tau=10$ ps. For Both: $R_1=R_2=R_3=C_{13}=0$, $C_L=6$ fF, driver width = 10 μm, load width = 5 μm.

first calculated from the two-dimensional program assuming 1-μm gate length, a donor value of $3\times10^{16}/cm^3$, an active layer thickness of 0.25 μm, and a built-in voltage of 0.5 V. The calculated drain–source current–voltage characteristics are shown in Fig. 11. The parameters necessary for SPICE 2 and R-CAP were than evaluated. Fig. 12 shows the results of circuit simulation by the three methods for a specific input (gate) voltage waveform. The two-dimensional result is taken to be the most exact. It can be seen that the result from SPICE 2 has errors in risetime, gain and propagation delay whereas the result using R-CAP is reasonably accurate. For example, the

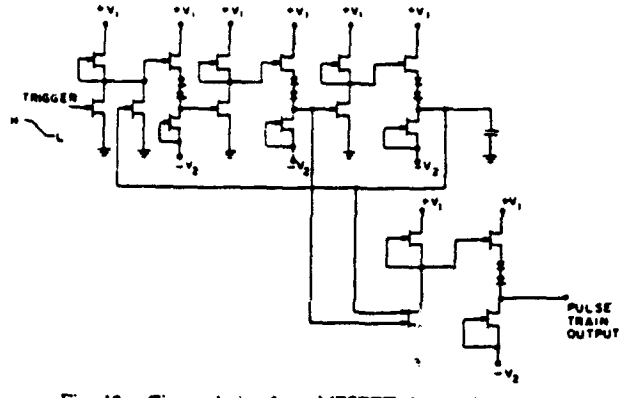

Fig. 13. Circuit design for a MESFET short-pulse generator.

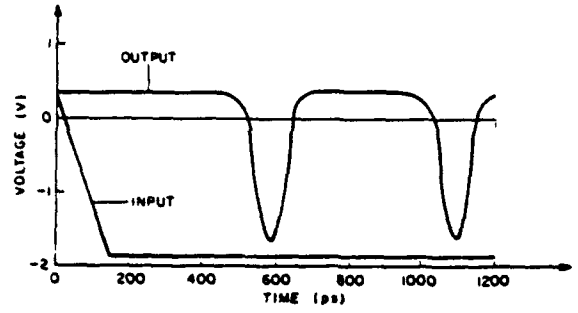

Fig. 14. Calculated output voltage as a function of time for MESFET pulse generator of Fig. 13 with $V_1 = 4$ V, $V_2 = 3$ V; MESFET. Constants are $\lambda = 0$, $\alpha = 2.3\ V^{-1}$, $V_T = 2.63$ V, $\beta = 26.3\ \mu A/\mu m$, $R_1 = R_3 = 0.15\ \Omega/\mu m$, $R_2 = 0.5\ \Omega/\mu m$, $\tau = 10$ ps, $V_{BI} = 1.0$ V, FET widths: Drivers = 100 μm, Load = 75 μm, source follower = 100 μm, source follower load = 75 μm, dual-gate FET widths: lower = 100 μm, upper = 150 μm, load capacitor = 0.5 pF, $C_{12} = 0.06\ fF/\mu m$, $C_{13} = 0.2\ fF/\mu m$.

gain predicted by SPICE 2 is 1.59 whereas R-CAP predicts 2.53 and the two-dimensional result is 2.38. The error in propagation delay for SPICE 2 is primarily related to the neglect of transient-time effects and the error in gain is due to the inability of the JFET model (in SPICE 2) to approximately the sharply saturating current–voltage characteristics of Fig. 11.

The second example is an IC design capable of producing triggerable bursts of short pulses. The goal was a half-width of 100 ps and MESFETs with a gain–bandwidth product of 15 GHz were to be used. The design developed is a triggerable ring oscillator with a NAND gate connected across two stages. Fig. 13 illustrates the circuit.

Fig. 14 shows the output pulse train as calculated by the R-CAP simulation program. It is seen that the final pulse width is about 77 ps which is well under the design goal of 100 ps. In addition, the circuit's output is not broadened by triggering with a slow input step, as shown. This is due to the high gain achieved by the FET inverter gates. The pulse train can be stopped by returning the input voltage to the high state.

The effect upon the output waveform produced by degradation of the individual MESFET's can be easily studied by further simulation.

V. Conclusion

A circuit model for the GaAs MESFET for use with time-domain circuit simulation programs has been described. The importance of accurately describing the drain current control characteristics, transit-time effects, gate capacitance, and circuit parasitics has been discussed. The parameters for the model must come from experimental measurements or from accurate detailed models, such as a two-dimensional internal model.

To illustrate the use of the model, an IC circuit design was simulated. It was shown possible to produce short pulses of less than 100 ps in a triggerable manner with an MESFET circuit. Such a circuit would be useful for timing purposes.

Acknowledgment

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GaAs FET Large-Signal Model and its Application to Circuit Designs

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Abstract—A large-signal GaAs FET model is derived based on dc characteristics of the device. Analytical expressions of modeled nonlinear elements are presented in a form convenient for circuit design. Power saturation and gain characteristics of a GaAs FET are studied theoretically and experimentally. An oscillator design employing the large-signal model is demonstrated.

I. Introduction

INFORMATION on the large-signal behavior of GaAs FET's is very limited. Often GaAs FET power amplifiers and oscillators are designed using small-signal S parameters, necessitating either tweaking of the circuits or cut and trys later to improve the circuit. In power amplifier design, the load pull method [1] is frequently used to obtain the optimum load condition at large-signal operation. However, this cannot predict gain performance of the designed circuit for small- or large-signal levels.

Willings *et al.* [2], [3] proposed a large-signal GaAs FET model by measuring bias dependence of small-signal S parameters and established expressions for an instantaneous equivalent circuit in terms of terminal voltages. They made it possible to predict large-signal performance such as power saturation and distortion at arbitrary input levels. Their use of time-domain analysis, however, is not always convenient for circuit design where frequency-domain elements, such as Ls and Cs, are commonly used. Also their expressions for equivalent circuit elements are based on S parameters measured at all the possible bias conditions the RF signal can sweep. This is not easy, especially when RF swing is large; for instance, when it swings into large drain voltage region or forward gate bias condition.

In this paper, we will first discuss the derivation of RF equivalent-circuit elements in terms of signal voltages, based on static characteristics of an FET, such as dc drain current–voltage curves, gate current–voltage curves, etc., all of which are parameters easy to obtain experimentally. Assuming sinusoidal variation to all the terminal voltages, nonlinear element values are obtained analytically with these curves built in as analytical functions. Thus nonlinear expressions for arbitrary size FET's can be calculated once these curves are determined by dc measurements.

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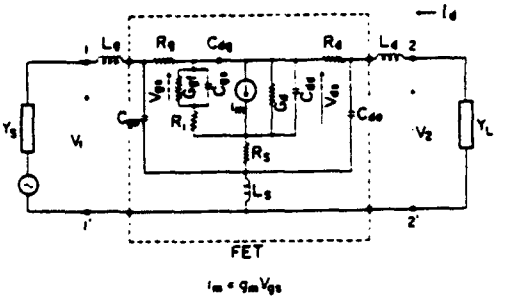

Fig. 1. FET equivalent circuit.

By connecting outside circuits to this nonlinear model, FET performance can be obtained consistently at any level from small signal to large signal. With this we studied power saturation and variation of the optimum load conditions, comparing our results with experimental data. An application of the nonlinear model to an FET oscillator design is also demonstrated. Available output power is mapped on a load impedance chart which gives a full description of an oscillating FET.

II. Large-Signal Equivalent Circuit

Under large-signal operation, element values of the FET equivalent circuit, shown in Fig. 1, vary with time because at large driving levels they become dependent on terminal voltages. We may consider two of the terminal voltages to be independent and choose the set V_{gs} and V_{ds}, V_{gs} being the voltage across the gate capacitance and V_{ds} across the drain conductance. If we restrict our interest to the signal frequency and ignore the effects due to higher harmonic components, these voltages can be written as

$$V_{gs} = V_{gs0} + v_{gs} \cos(\omega t + \phi) \tag{1}$$

$$V_{ds} = V_{ds0} + v_{ds} \cos \omega t \tag{2}$$

where V_{gs0} and V_{ds0} are the dc bias voltages, v_{gs} and v_{ds} amplitudes of signal frequency components, and ϕ the phase difference between gate and drain voltages. The equivalent circuit for the signal frequency can now be expressed as a function of the following parameters which are independent of time: V_{gs0}, V_{ds0}, v_{gs}, v_{ds}, ω, and ϕ.

In order to avoid unnecessary complexity of calculations, we limit the nonlinear behavior to five elements, gate forward conductance G_{gf}, gate capacitance C_{gs}, gate charging resistance R_i, transconductance g_m, and drain conductance G_d. Here, G_{gf} represents the effect of the forward rectified current across the gate junction under large-signal operation. No volt-

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age dependence was assumed for parasitic elements, i.e., lead inductances (L_g, L_d, L_s), contact resistances (R_g, R_d, R_s), and pad capacitances (C_{ge}, C_{de}). We also ignored the voltage dependence of drain channel capacitance C_{ds} and feedback capacitance C_{dg} due to their small values.

A. Expressions for g_m and G_d

Transconductance g_m and drain conductance G_d are defined as

$$g_m = \left(\frac{i_{ds}}{v_{gs}}\right)_{v_{ds}=0} \qquad G_d = \left(\frac{i_{ds}}{v_{ds}}\right)_{v_{gs}=0} \tag{3}$$

where i_{ds} is the RF drain current amplitude. The instantaneous drain current can be written using g_m and G_d as

$$I_{ds}(t) = I_{ds0} + g_m v_{gs} \cos(\omega t + \phi) + G_d v_{ds} \cos \omega t \tag{4}$$

where I_{ds0} is the dc drain current. In this expression linear superposition of two terms is assumed.

Now, if we have a function which can simulate drain current I_{ds} as a function of V_{gs} and V_{ds}, as

$$I_{ds} = I_{ds}(V_{gs}, V_{ds}) \tag{5}$$

instantaneous current $I_{ds}(t)$ can be obtained by inserting (1) and (2) into (5). By multiplying $\sin \omega t$ to (4) and integrating over a complete period, g_m is obtained as

$$g_m = -\frac{\omega/\pi}{v_{gs} \sin \phi} \int_0^{(2\pi/\omega)} I_{ds} \sin \omega t \, dt. \tag{6}$$

Similarly, G_d is obtained as

$$G_d = \frac{\omega/\pi}{v_{ds} \sin \phi} \int_0^{(2\pi/\omega)} I_{ds} \sin(\omega t + \phi) \, dt. \tag{7}$$

Equations (6) and (7) are now functions of RF amplitudes v_{gs} and v_{ds}, as well as bias voltages V_{gs0} and V_{ds0}.

The equation for I_{ds} was arrived at empirically to simulate the typical dc transistor curves. Any other function that reproduced the I-V behavior could have been used.

$$I_{ds}(V_{ds}, V_{gs}) = I_{d1} \cdot I_{d2}$$

$$I_{d1} = \frac{1}{k}\left[1 + \frac{V'_{gs}}{V_p} - \frac{1}{m} + \frac{1}{m} \exp\left\{-m\left(1 + \frac{V'_{gs}}{V_p}\right)\right\}\right]$$

$$I_{d2} = I_{dsp}\left[1 - \exp\left\{\frac{-V_{ds}}{V_{dss}} - a\left(\frac{V_{ds}}{V_{dss}}\right)^2 - b\left(\frac{V_{ds}}{V_{dss}}\right)^3\right\}\right]$$

$$k = 1 - \frac{1}{m}\{1 - \exp(-m)\}$$

$$V_p = V_{p0} + pV_{ds} + V_\phi$$

$$V'_{gs} = V_{gs} - V_\phi \tag{8}$$

where $V_{p0}(>0)$ is the pinchoff voltage at $V_{ds} \sim 0$, V_{dss} is the drain current saturation voltage, V_ϕ is the built-in potential of the Schottky barrier, I_{dsp} is the drain current when $V_{gs} = V_\phi$, and a, b, m, and p are fitting factors that can be varied from device to device.

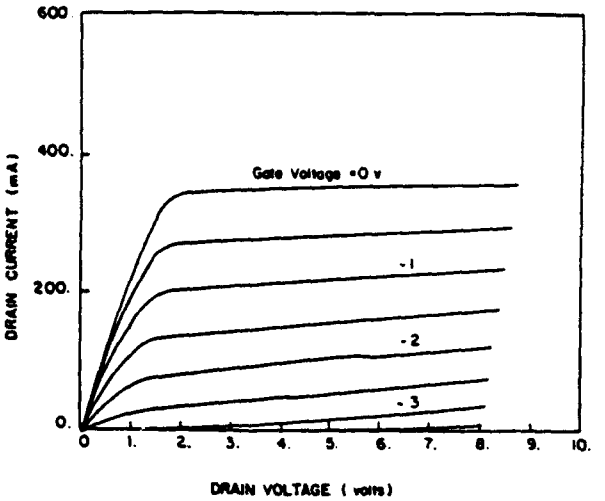


Fig. 2. I_D-V_D characteristics calculated from (8) with parameter values of Table I, column a.

TABLE I
ELEMENT VALUES OF THE FET EQUIVALENT CIRCUIT AND BIAS CONDITIONS
(Values in column a are for the amplifier, in column b for the oscillator)

	a	b		a	b
i_s(pA)	3	0.15	α(1/V)	30	30
C_{gso}(pF)	0.3	0.4	τ_i(ps)	3	2
I_{dsp}(mA)	70	55	V_{po}(V)	2	2.0
V_{dss}(V)	0.7	1			
R_g(Ω)	3	4	R_d(Ω)	3	4
R_s(Ω)	3	3	L_s(nH)	0.02	0.05
L_g(nH)	0.15	0.3	L_d(nH)	0.15	0.3
C_{ge}(pF)	0.01	0.02	C_{de}(pF)	0.01	0.02
C_{dg}(pF)	0.015	0.01	C_{ds}(pF)	0.02	0.02
a	-0.2	-0.2	m	3	3
b	0.6	0.6	p	0.2	0.2
C_F(pF)	---	10	L_F(nH)	---	1.5
t_g(mm)	---	0.7	t_d(mm)	---	0.7
V_{dso}(V)	7	5	V_{gso}(V)	-1	-0.4

Drain current versus voltage curves shown in Fig. 2 were obtained from (8) when these parameters were given as in Table I(column a).

B. Nonlinear Expressions for C_{gs}, G_{gf}, and R_i

Although the gate junction is also a function of V_{gs} and V_{ds}, we assumed here that it can be approximated by a Schottky-barrier diode between gate and source, with V_{gs} as the sole voltage parameter. Gate capacitance C'_{gs} and forward gate current i_{gf} can be found from Schottky-barrier theory as

$$C'_{gs} = C'_{gso}/\sqrt{1 - V_{gs}/V_\phi} \qquad (-V_p \leqslant V_{gs}) \tag{9}$$

or

$$C'_{gs} = C'_{gs0}/\sqrt{1 + V_p/V_\phi} \quad (-V_p \geq V_{gs})$$
$$i_{gf} = i_s (\exp \alpha V_{gs} - 1) \tag{10}$$

where C'_{gs0} is the zero bias gate capacitance, i_s the saturation current of the Schottky barrier, and $\alpha = q/nkT$.

When V_{gs} varies according to (1), effective gate capacitance C_{gs} and gate forward conductance G_{gf} for the signal frequency are obtained from (1), (2), (9), and (10) as

$$C_{gs} = \frac{1}{\pi v_{gs}} \int_0^{2\pi} \left(\int^{V_{gs}} C'_{gs}\, dV \right) \cos \omega t\, d(\omega t) \tag{11}$$

$$G_{gf} = 2 i_s \exp(\alpha V_{gs0})\, I_1(\alpha v_{gs})/v_{gs} \tag{12}$$

where $I_1(x)$ is the first-order modified Bessel function.

Gate charging resistance R_i was assumed to vary in such a way that the charging time constant did not change [4]

$$R_i \cdot C_{gs} = \tau_i \text{ (constant)}. \tag{13}$$

III. Amplifier Design

The device under analysis is based on an arbitrarily selected GaAs FET which had a 0.7-μm gate with 250-μm width. Nonlinear element parameters and parasitic element values are listed in Table I (column a).

Available output power of the device was calculated as a function of input power following the procedure described below.

By giving a driving RF voltage for v_{gs}, output voltage v_{ds} and phase shift ϕ are calculated assuming some initial values for nonlinear elements and signal and load admittances, Y_S and Y_L. Knowing v_{gs}, v_{ds}, and ϕ, nonlinear element values are revised according to (6), (7), (11), (12), and (13). The revised equivalent circuit with new element values determines a new value for v_{ds} and ϕ, which will again change the nonlinear element values. When this process converges, the equivalent circuit is obtained for the driving level of v_{gs}. From terminal voltages, v_1 and v_2, input and output powers P_1 and P_2 are calculated using admittances Y_S and Y_L.

The operating condition is dependent on terminating admittances Y_S and Y_L. Fig. 3 shows calculated saturation output power contours plotted on the load admittance chart. Source admittance Y_S was kept matched to the device input admittance as it varied with input power and Y_L. The figure shows the maximum power condition and saturation power rolloff as the load mismatches to the optimum load. Also shown in the figure are experimental data taken with known admittances while the input circuit was tuned for best output power. Considering the difficulty of measuring admittances, the agreement is very good.

Fig. 4 shows theoretical and experimental power gain performance for three different terminations. Although a small discrepancy in saturation power is found, the general dependence of small-signal gain and saturation power on termination admittance is successfully simulated. The discrepancy in saturation power could be due to gate-drain breakdown, which is not modeled in the calculation. The saturation mechanism of the model can be seen in Fig. 5, which shows variation of

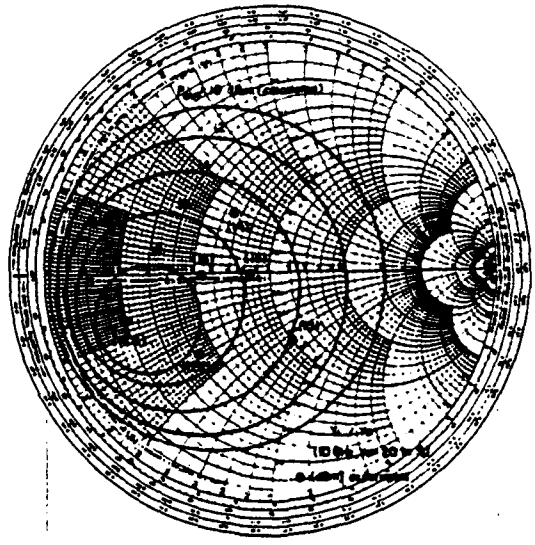


Fig. 3. Saturation power contours on load admittance chart.

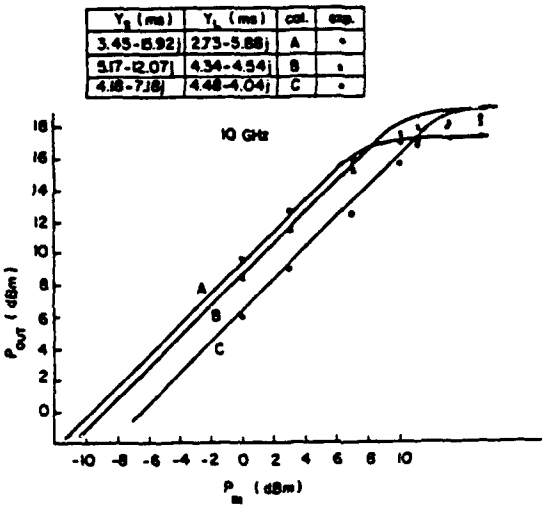


Fig. 4. Variation of gain with terminating impedance.

the nonlinear element values as a function of input power. Although C_{gs}, R_i, g_m, and G_d change a small amount, the increase of G_{gf} is significant in the saturation region. In other words, saturation of output power is caused by rectified current across the gate junction. This limits input power by increasing loss in the circuit resistances as power increases.

Using the model, output power performance of GaAs FET amplifiers can be simulated at arbitrary input levels and terminating impedances. The calculations provide predictions of both small-signal gain and saturation power necessary to circuit designers.

IV. Oscillator Design

Although we discuss here an oscillator circuit using a common source FET with a feedback circuit embedded between gate and drain, the calculation method is feasible for any other circuit topologies of oscillators.

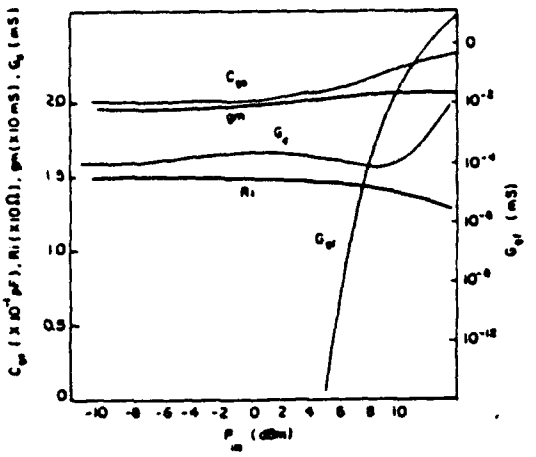


Fig. 5. Variation of nonlinear element values with input power.

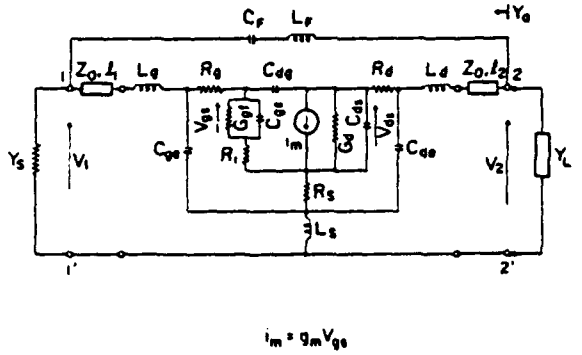


Fig. 6. FET oscillator equivalent circuit.

The equivalent circuit of an FET in an oscillating circuit is expressed by the same equivalent circuit as an amplifier except that a feedback circuit, composed of C_F and L_F, is now placed between the gate and drain ports (Fig. 6). Distances between the actual ports and feedback points are expressed by lengths l_1 and l_2 of transmission lines of impedance Z_0. The gate port is terminated by 20 mS(Y_s) for the purpose of stabilizing the circuit [5].

Large-signal behavior of the device was calculated following a procedure similar to that described in the previous section. Parameters used to model a 400 × 1 μm gate FET are listed in Table I(column b) for a bias condition of -0.4-V gate, 5-V drain. Variation of oscillating device admittance Y_a was obtained as a function of available output power P_2 which was calculated from terminal voltage v_2 and the real part of Y_a. Loci of Y_a, shown in Fig. 7, revealed a complete map of the available power and frequency within the unstable region of the device. This particular circuit has an optimum oscillating frequency around 9 GHz with a maximum output power of 35 mW and efficiency of 25 percent when load Y_L is $(6 + 4j)$ mS. With this knowledge, an oscillator can be designed at its optimum.

This calculation was confirmed by the circuit shown in Fig. 8. A GaAs FET was mounted between two microstrip

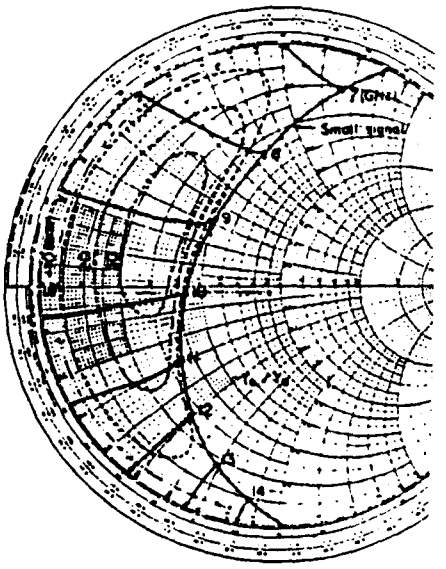


Fig. 7. Calculated oscillating device admittance for increasing values of available output power.

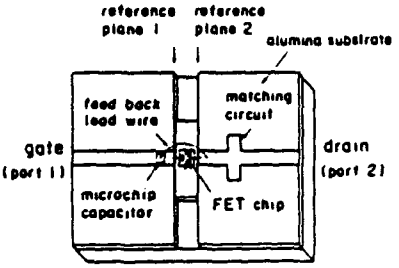
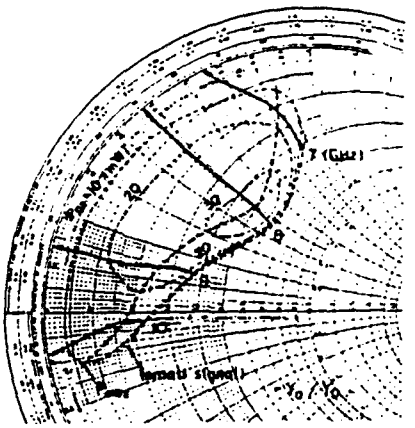


Fig. 8. FET oscillator circuit.



V_{dso} = 5V
V_{gso} = -0.4V
Y_0 = 20mS

Fig. 9. Measured oscillating device admittance.

circuits with a feedback circuit between drain and gate constructed by a lead wire and a microchip capacitor. The gate port was terminated by 50 Ω.

Device admittance Y_d was measured at the drain port (reference plane 2) and is shown in Fig. 9 which has the same pattern as the calculated results in Fig. 7. With a matching circuit designed to convert the optimum admittance to the 50-Ω load, the circuit operated as an oscillator. Its output power and oscillation frequency at the optimum bias condition were 30 mW and 8.8 GHz, very close to predicted data.

V. Conclusion

A technique to model the large-signal behavior of GaAs FET's was proposed. Because the model was derived based on dc current-voltage characteristics, it was easy to apply to any arbitrary size FET once its dc curves were given. By limiting our interest to the fundamental frequency of the signal, it was possible to analyze the circuit in the frequency domain rather than the time domain. Device analysis and circuit simulation have thus become simple enough for use in circuit design.

The model was used to study power performance of FET's. Output-power saturation values were predicted and confirmed by experiment. Because the terminating impedances of the circuit can be varied, the model is useful for predicting power performance of GaAs FET amplifiers.

By applying a feedback element to the nonlinear model of an FET, oscillatory behavior of the FET was studied. A complete admittance chart with available power and frequency in the unstable region of the device was calculated and confirmed by experimental data. The chart provided complete data for designing an oscillator at maximum efficiency.

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Single-Gate MESFET Frequency Doublers

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Abstract—A simple analytic model of the FET frequency doubler is used to determine the relative contributions of the various nonlinearities to harmonic generation. FET doubler conversion gain and its variation with frequency relative to the fundamental frequency available gain is also estimated. Large-signal computer simulations are used to determine the validity of the analytic model and provide further information on conversion gain and its frequency dependence. The analytic and computer predictions are compared with experimental measurements on a 4- to 8-GHz single-gate FET frequency doubler.

I. Introduction

GaAs MESFET'S operated as frequency multipliers are attractive because they provide conversion gain over a broad frequency band and also have some isolation between the input and output ports. In the GaAs monolithic integrated circuit context, the fabrication of FET multipliers is preferable to the processing of p-n junction varactor or Schottky-diode multipliers in the presence of other FET circuits. Hence, there is considerable interest in FET harmonic generators at the present time.

Experimental results on both single- and dual-gate FET frequency multipliers have been published [1]–[5] and limited results are available from a computer simulation of a single-gate FET multiplier [4]. The object of the present paper is to determine the relationship between the conversion gain of the single-gate FET frequency doubler and the fundamental frequency gain of the device and also predict its frequency limitations.

Simple analytic considerations of the single-gate FET determine the relative contributions of the various nonlinearities to harmonic generation. Based on these, the FET frequency doubler conversion gain and its frequency variation is related to the device fundamental frequency gain. Computer simulations, initially using a unilateral model and subsequently a more complex but realistic model, examine the validity of these results. Experimental measurements on a 4–8-GHz doubler using a commercial medium power *C*-band FET (MSC88001) are compared with simulation results to determine the accuracy of the large-signal computer model.

II. Theoretical Considerations

The equivalent circuit in Fig. 1 is considered as representative of a common-source medium-power single-gate FET. The parameter values of the circuit elements in this figure title are those of a commercial medium power *C*-band FET (MSC 88001), estimated from small-signal scattering parameter measurements. The I_{ds}–V_{ds} characteristics of this device related to this model are given in Fig. 2. Note that the curves are an approximation to the measured characteristics of this device in that the output conductance always remains positive. The use of these characteristics makes the calculations quasi-static. The parameters for these curves give a pinchoff voltage V_p of -6 V, and an I_{ds} of 180 mA for 0-V gate bias and V_{ds} of 5 V. The straight line portions of these characteristics are given by

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2\left(1 + \frac{V_{ds}}{R_{do} I_{dss}}\right) \qquad (1)$$

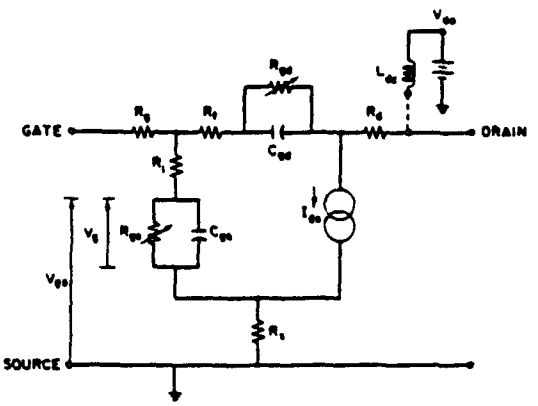

Fig. 1. Equivalent circuit for the MSC 88001 FET in the grounded source configuration. For the transistor used in the simulations the parameters are $R_g = R_d = 0\ \Omega$, $R_i = 26\ \Omega$, $R_f = 28\ \Omega$, $R_s = 1\ \Omega$, $C_{gso} = 0.47$ pF, $C_{gdo} = 0.25$ pF. Note that the bias circuit is removed when the device is used with the load circuit of Fig. 3(b).

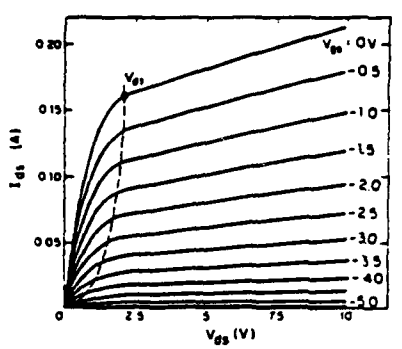

Fig. 2. I_{ds}–V_{ds} characteristics for the device in Fig. 1.

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where I_{dss} is the drain-source saturation current; V_{ds} is the drain-source voltage; V_{gs} is the gate-source terminal voltage; R_{do} is the output conductance; and V_p is the gate pinchoff voltage. The curved sections of the characteristics are cubics, chosen to become tangential to the above straight lines along a parabola which passes through the origin and intersects the 0-V bias line at V_{ds}, as shown in Fig. 2. The full expression for these characteristics is given in the Appendix. The simplified model calculations use (1) as the $V_{gs}-I_{ds}$ transfer characteristic with R_{do} assumed to be large.

The major nonlinearities in the FET causing harmonic generation are: 1) the gate-source and gate-drain nonlinear capacitors C_{gs} and C_{gd}, which represent the gate-junction depletion layer capacitance [6]; 2) the drain current I_{ds} nonlinearity, which arises when the current is clipped when V_{gs} swings below pinchoff and/or swings positive to cause the gate diode, represented by R_{gs}, to conduct; 3) the nonlinearity of the $V_{gs}-I_{ds}$ transfer characteristic, which in the present instance is assumed to be quadratic, as given by (1) and (A.1), but in practice is more complex; and 4) the output conductance nonlinearity. The contributions of each of these are included in the calculations.

III. Simplified Analysis

The calculations in this section omit the gate-drain branch of the equivalent circuit (see Fig. 1), and assume that $R_s = 0$, that the load is resistive and that the $V_{gs}-I_{ds}$ transfer characteristic is given by (1), unless specified otherwise, and holds over the whole positive $I_{ds}-V_{ds}$ quadrant. Omission of the gate-drain branch is an acceptable approximation since the capacitance C_{gd} becomes small over the relevant range of biasing conditions.

A. Effect of Gate-Source Capacitor

The input capacitor C_{gs} and series resistance R_i, of the gate-source junction can be analyzed as a lossy varactor diode. The FET gate-source capacitance at 0-V bias is $C_{gs0} = 0.47$ pF, and the series resistance $R_i = 26\ \Omega$, and therefore the zero bias cutoff frequency of the diode is about 13 GHz. The second harmonic voltage generated across the capacitor from voltage-driven elastance calculations [7], [8] is approximately 12–30 percent of the fundamental, depending on the value of breakdown voltage chosen. In the absence of other nonlinearities, this result suggests that the second harmonic level due to the nonlinearity is of the order of -18 to -11 dB relative to the fundamental.

B. Effect of I_{ds} Clipping Nonlinearity

When the FET is biased close to 0 V, just below the forward conduction point of the gate-source junction, the voltage waveform across the gate-source capacitor is clipped due to junction conduction. The waveform takes the half-wave rectified form, assuming that the negative maximum does not reach pinchoff, and is transferred to I_{ds} through the transfer characteristic. Fourier analysis of the half-wave rectified form gives a fundamental voltage component magnitude of $V/2$ and a second harmonic voltage magnitude of $(2V/3\pi)$. Neglecting the transfer characteristic nonlinearity, the second harmonic output power level is 7.4 dB below the fundamental component.

When the device is biased at the pinchoff voltage, the drive voltage causes the FET to be turned on only during the positive half-cycles of the drive waveform. The output waveform would again take the near half-wave rectified form, assuming that the gate voltage did not rise to the forward conduction point. Neglecting the nonlinear transfer characteristic, a similar value of second harmonic level would be obtained. In a practical FET, the transfer characteristic is nonlinear, and the transconductance g_m falls off as pinchoff is approached. However, since the average value of C_{gs} becomes lower at the more negative bias, this fall in g_m may be offset by the increase in voltage swing across C_{gs}, causing an increase in gain [5].

C. Effect of $V_{gs}-I_{ds}$ Transfer Characteristics and Output Conductance

The transfer characteristic in (1) may be simplified to

$$I_{ds} = I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2 f(V_{ds}, R_{do}). \tag{2}$$

For the present, $f(V_{ds}, R_{do})$ is assumed to be constant. A sinusoidal excitation for V_{gs} of the form $(V_0 + V_1 \sin \omega t)$ gives rise to the following terms (assuming no clipping occurs):

$$I_{ds} = I_{dss}\left[\left\{\left(1+\frac{V_0}{V_p}\right)^2 + \frac{V_1^2}{2V_p^2}\right\} - 2\left(1-\frac{V_0}{V_p}\right)\frac{V_1}{V_p}\sin\omega t - \frac{V_1^2}{2V_p^2}\cos 2\omega t\right]. \tag{3}$$

The ratio of the second harmonic to fundamental current magnitudes at the current generator is given by

$$\left|\frac{I_{2f}}{I_f}\right| = \left|\frac{V_1}{4V_p\left(1-\frac{V_0}{V_p}\right)}\right|. \tag{4}$$

For $V_p = -6$ V, the gate biased at midpoint, so that $V_0 = -3$ V and $V_1 = 3$ V, this ratio becomes 1/4. Therefore, the second harmonic level due to this nonlinearity is approximately 12 dB below the fundamental.

Inclusion of the output conductance nonlinearity is effected by allowing the term $f(V_{ds}, R_{do})$ in (2) to vary. Suppose the load circuit comprises a resistance, R_l, in shunt with a RF choke, fed from a drain supply of voltage V_{d0}, giving rise to an average current of I_{d0} (see Fig. 3(b)). Then

$$V_{ds} = V_{d0} - (I_{ds} - I_{d0})R_l. \tag{5}$$

Assuming a sinusoidal excitation for V_{gs} for the form $(V_0 + V_1 \sin \omega t)$, as above, and substituting in (1) and (5)

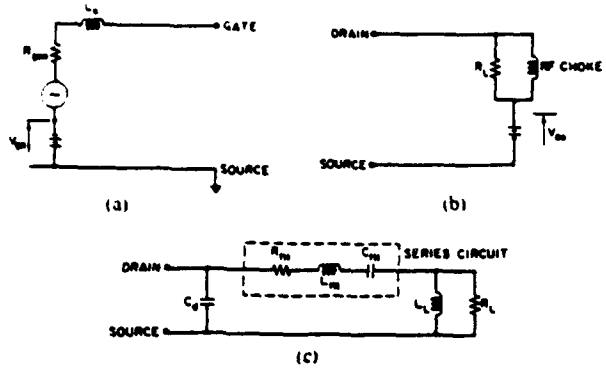

Fig. 3. Input and output circuits for FET. (a) Input circuit. (b) Resistive load circuit. (c) Tuned load circuit. Series circuit is resonant at $2f$ and C_d and L_d are parallel resonant at $2f$ for doubler operation. Note the new drain bias circuit with resistive load in (b).

gives

$$I_{ds} = \frac{\left(1 - \dfrac{V_0 + V_1 \sin \omega t}{V_p}\right)^2 \left(\dfrac{V_{d0} + I_{d0} R_l}{R_{do}} + I_{dss}\right)}{1 + \left(1 - \dfrac{V_0 + V_1 \sin \omega t}{V_p}\right)^2 \dfrac{R_l}{R_{do}}}. \quad (6)$$

Simplifying this for a wide range of parameters is difficult. For $R_l \ll R_{do}$, the results of (4) are approximately valid, but for other values of R_l the level of the second harmonic component relative to the fundamental has to be estimated numerically.

When the bias point approaches pinchoff or gate forward conduction, the waveform in the above expression (6) for $V_1 \sin \omega t$ has to be modified to include the clipping effect. The simplification of the expression derived from (6) also becomes difficult, and therefore the analysis is computed as described in Section IV.

D. Results of Analysis

Based on the above discussions, the FET doubler has a peak in conversion gain (or minimum conversion loss) with the gate biased close to 0 V or pinchoff, and this would be about 6 to 8 dB below the corresponding fundamental frequency gain. At gate bias midway between these extremes, the conversion gain is expected to drop a further 4–6 dB relative to the fundamental gain. These figures will be modified somewhat at high drive levels.

In the absence of transit time effects, the fundamental frequency gain of the device falls at 6-dB octave, and the second harmonic gain, which is about 6–8 dB less than the fundamental gain, also falls at the same rate. This suggests that second harmonic conversion becomes lossy as the doubler output frequency approaches the device small-signal unity-gain frequency f_T.

IV. Computer Large Signal Modeling

The nonlinear behavior of the FET cannot be easily characterized, as seen above, and therefore computer modeling is the only means of completely analyzing the FET doubler. The modeling predicts FET doubler performance and also determines the validity of the simple analytic results in Section III.

The large-signal model in the present simulation uses the FET equivalent circuit shown in Fig. 1, and input and load circuits as in Fig. 3. The transfer characteristics for the particular load circuit trajectory are determined from the I_{ds}–V_{ds} characteristics in Fig. 2 for known values of V_{gs} and V_{ds}. The circuit model together with its characteristics are analyzed in the time domain by integration of appropriate differential equations.

The equivalent circuit model represents the gate depletion-layer as two nonlinear capacitors each shunted by nonlinear resistors. The variation of the gate–source capacitor with voltage is given by

$$C_{gs} = C_{gs0}\left(1 - \frac{V_g}{V_{bi}}\right)^{-1/2} \quad (7)$$

where C_{gs0} is the gate–source capacitance at 0-V gate bias; V_g is the voltage across the capacitor; and V_{bi} is the built-in gate—source junction voltage. The nonlinear resistor R_{gs} represents the gate–source junction, and the conduction current through it is given by

$$I_{gs} = I_{gs0}(\exp \alpha V_g - 1) \quad (8)$$

where I_{gs0} is the leakage current through the junction $\alpha = q/nKT$, where n is the ideality factor of the junction, equal to unity in these calculations.

Similarly, C_{gd} and R_{gd} represent the gate–drain junction and their values are determined from equations similar to (7) and (8), with the gate–drain voltage V_{gd} as the independent variable. The output conductance at the current generator is included in the characteristics in Fig. 2 and (A.1) and therefore is not specified in the output circuit. The bias circuit is omitted from Fig. 1 when the resistive load circuit in Fig. 3(b) is used. Package and device parasitics have been omitted, with the exception of C_d in Fig. 3(c), because they increase the complexity of the simulation and do not contribute to the physical mechanisms of harmonic generation.

Time-derivative differential equations for currents and voltages are set up for the appropriate model including the input and load circuits, and integrated using the Gear [9] routine. The current generator I_{ds} is determined from the values of V_{ds} and V_{gs} in (A.1). Note that V_{gs} includes the voltage across C_{gs} and R_s, since the characteristics in Fig. 2 are derived from the static characteristics which retain this drop. Omission of the R_s drop from V_{gs} only changes the results by a few percent.

The gate transit time τ varies with V_{gs}, but for simplicity may be approximated by a constant value which is the gate length divided by the saturated velocity ($\sim 10^7$ cm/s). In the time domain its effect is accounted for by averaging the value of V_{gs} over the past time period τ when estimating the drain current I_{ds}. However, for the present simulations, the transit time effect was omitted as it was thought that the computational time would increase considerably. The transit time effect becomes important as input and output

frequencies approach $f_t = 1/\tau$; however, the frequency f_t is much higher than those considered here.

The simulations use two models, a simple unilateral FET with a resistive load model, in which the various nonlinearities are introduced in sequence, and the complete model, which uses a tuned load circuit. Input current and voltage waveforms and similar output waveforms across the load resistor are Fourier analyzed to estimate the dc, fundamental, and harmonic components.

A. Unilateral Model

This model omits the gate–drain branch, which makes the device unilateral, and also omits the source resistance R_s. It is assumed that the input circuit (as in Fig. 3(a)) comprises the RF source, the gate-bias source, the generator resistance which matches the gate resistance, and a series inductor which matches the gate–source capacitor. The load circuit, as in Fig. 3(b), is a resistive load shunted by a large inductor (which is a short circuit at dc and an open circuit at RF), and the drain bias is connected through this circuit.

Simulations were performed in four cases, with increasing numbers of nonlinearities. Each case assumes that I_{ds} clipping occurs and also that C_{gs} is constant, determined by the dc gate bias as per (7), with a perfect diode across it, except in case (*iv*). These simulations are: (*i*) with $V_{gs}-I_{ds}$ linear characteristics; (*ii*) with the $V_{gs}-I_{ds}$ quadratic form as in 2(b), with $f(V_{ds}, R_{d0})$ set to unity; (*iii*) with the characteristics including the output conductance variation as in (A.1); and (*iv*) with C_{gs} varying as per (7), with gate–source junction current given by (8), characteristics as in (*iii*).

The parameters used in these computations are summarized in Table I. Fig. 4(a) and (b) show typical results of the variation of doubler gain against V_{gs} for an input frequency of 4 GHz with this model. Fig. 4(a) illustrates doubler behavior at a low input power (6.8 dBm). All curves here show that the conversion gain peaks near 0-V gate bias and near pinchoff as predicted in Section III. The midpoint bias minimum doubler gain position is present in all curves, but their position varies with the nonlinearities included. The minimum is about 15 dB below the doubler gain peak in case (*iv*) above and even lower in the other cases. The linear characteristic case (*i*) shows a second minimum as a consequence of the increase in C_{gs} with bias reducing the effect of I_{ds} clipping.

The overall doubler gain curve shape changes from the linear characteristic case (*i*), when the quadratic characteristics in (*ii*) are used. There is little change in the results when the output conductance variation is also included in (*iii*). Inclusion of the C_{gs} variation with V_{gs}, and the gate–source junction current, in (*iv*) changes the curve shape by reducing the negative value at the minimum and by moving its position towards pinchoff. The variation of C_{gs} with V_{gs} also increases the peak gain by 1 or 2 dB, confirming that the contribution of this nonlinearity is small. Thus, the I_{ds} clipping nonlinearity is the major contributor to harmonic generation, with additional contributions from the transfer nonlinearity and the C_{gs} nonlinearity. The peak of the doubler gain, however, is about 10 dB below the corresponding fundamental frequency gain close to 0-V bias and pinchoff, and the minimum in case (*iv*) is almost 22 dB below the corresponding fundamental frequency gain.

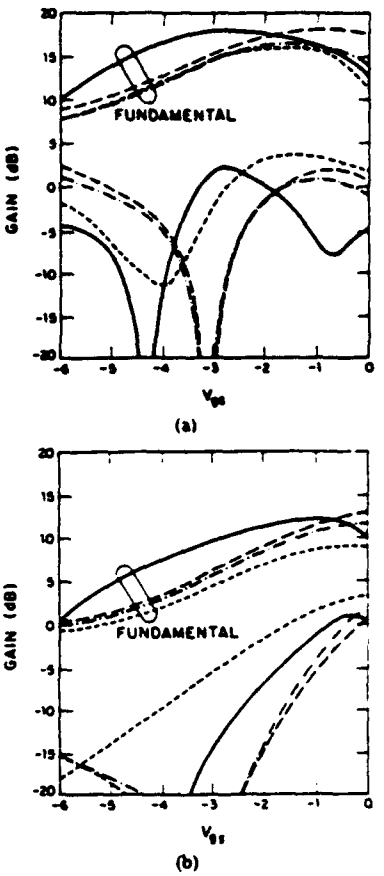

Fig. 4. Simulation results for a 4- to 8-GHz FET doubler as a unilateral device with (a) 6.8-dBm input and (b) 16.4-dBm input power. $V_{ds} = 5$ V. (*i*)——— linear $V_{gs}-I_{ds}$. (*ii*)— — —quadratic $V_{gs}-I_{ds}$. (*iii*)— · — · — $I_{ds}-V_{ds}$ characteristics. (*iv*)- - - C_{gs} varies with instantaneous gate voltage.

The results in Fig. 4(b) are at the higher input drive of 16.4 dBm at 4 GHz, and the patterns show considerable differences from Fig. 4(a). The linear characteristic case (*i*) shows large doubler conversion loss when biased near pinchoff, because the small value of C_{gs} causes the drain current waveform to become near square wave in form as a result of clipping due to both pinchoff and gate conduction. As the gate bias is increased towards 0 V, the waveform becomes asymmetric leading to an increase the second harmonic content. The curve shapes with the quadratic characteristics in (*ii*) and output conductance in (*iii*) are similar, except that the quadratic nonlinearity increases the second harmonic near pinchoff. The minimum gain in these cases is higher than the linear characteristics case (*i*). The effect of output conductance nonlinearity is again seen to be small.

When the C_{gs} variation with drive is included, the peak

TABLE I
THE PARAMETERS USED IN THE FOUR CASES OF THE UNILATERAL MODEL SIMULATION: $V_{g,0}$ IS THE DC BIAS OF THE GATE

Case No.	I_{ds} Relationship	C_{gs} Variation	Gate-Source Junction Current
(i)	constant x V_{gs}	$C_{gso}\left(1-\frac{V_{gso}}{V_{bi}}\right)^{-1/2}$	0
(ii)	$I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2$	$C_{gso}\left(1-\frac{V_{gso}}{V_{bi}}\right)^{-1/2}$	0
(iii)	$I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2\left(1+\frac{V_{ds}}{R_{do}I_{dss}}\right)$ and associated cubics as in Eq. (A.1).	$C_{gso}\left(1-\frac{V_{gso}}{V_{bi}}\right)^{-1/2}$	0
(iv)	$I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2\left(1+\frac{V_{ds}}{R_{do}I_{dss}}\right)$ and associated cubics as in Eq. (A.1)	$C_{gso}\left(1-\frac{V_{gs}}{V_{bi}}\right)^{-1/2}$	$I_{gso}(e^{\alpha V_{gs}}-1)$

value of doubler gain near 0-V bias increases by about 2 dB, increasing to this value monotonically from minimum gain at pinchoff. In this case, the increased drive causes the waveform to become near square wave at biases near pinchoff, with increasing asymmetry as bias is moved towards 0 V. This appears to be the cause of the doubler gain curve shape seen in this Fig. 4(b) for case (*iv*).

Note that with large drive, the highest doubler gain occurs near 0-V bias and is about 6 dB below the corresponding fundamental frequency gain, as predicted earlier.

B. Full Model Simulation

This simulation uses the full equivalent circuit in Fig. 1, including the gate–drain series resistance and capacitor with its shunt diode, and the source series resistance R_s. The model is more representative of practical FET's; it allows negative excursions of the drain voltage by postulating similar characteristics as in Fig. 2 in the negative I_{ds} and V_{ds} third quadrant with V_{gd} as the controlling voltage. Breakdown at the junctions has not been included in the model and therefore predictions of device power handling capability are optimistic.

Selection of the value of C_{gd} is difficult. The results of Willing, Rauscher, and deSantis [6] suggest that C_{gd} does not fall according to the conventional abrupt junction variation with voltage given by

$$C_{gd} = C_{gd0}\left(1-\frac{V_{gd}}{V_{bi}}\right)^{-1/2} \tag{9}$$

Other authors [10] suggest that C_{gd} is purely parasitic and that any variation with voltage V_{gd} can be neglected. It would seem that this capacitor is a combination of the parasitic and part of the gate depletion layer capacitance, with the latter becoming small because of the drain bias. The variation of this part of the depletion layer capacitance would logically seem to follow the form in (9) above, with the inclusion of a factor to account for the geometric effect. However, the value of C_{gd0} for the present case was taken to be lower than the value of C_{gs0} without any geometric factor, and the parasitic capacitance was not included. The value chosen for C_{gd0} for these particular simulations is about half C_{gs0}, since this allows the C_{gd} variation to approach that predicted by Willing *et al.* [6]. The variation of the C_{gd} with voltage also contributes to the device nonlinearity, but in general this is not a significant factor in harmonic generation because of the large negative bias across it, and large value of associated series resistor.

Some results of the computation for a 4- to 8-GHz doubler, are given in Fig. 5, which is a plot of doubler conversion gain against gate-bias voltage for two different values of input power. Results at lower input powers have been omitted for clarity, since these follow similar trends. Included in this figure are the experimental results for a 4- to 8-GHz doubler, which are discussed below. Note the good agreement between the simulation and experiment. Fig. 6 shows both fundamental gain and doubler conversion gain as a function of RF input power, for different input frequencies at 0-V gate bias. The fundamental gain falls at 6 dB/octave at low input power, and the doubler gain also falls in a similar fashion, but is input-power dependent. Note that doubler conversion gain is negative at input frequencies above 4 GHz.

The full simulation has been performed with a specific circuit topology and circuit parameters. The results show

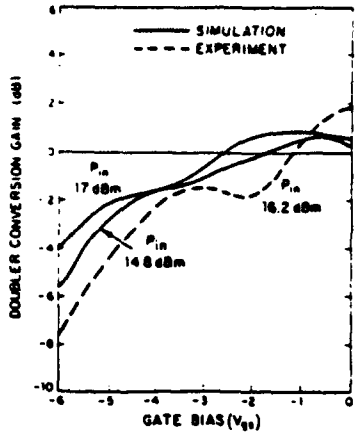

Fig. 5. Simulation results for a 4- to 8-GHz FET doubler using the full equivalent circuit model for input powers of 14.8 dBm and 17 dBm. Experimental results on the MSC 88001 device for an input power of 16.2 dBm is also shown for $V_{ds} = 5$ V, $V_{gs} = 0$ V.

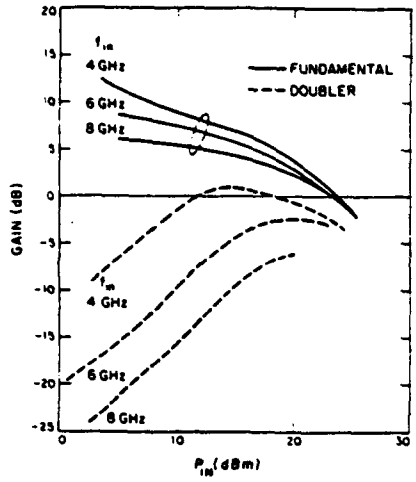

Fig. 6. Simulation results showing fundamental and doubler gain for the FET doubler using the full equivalent circuit for input frequencies of 4, 6, and 8 GHz, as a function of input power, for $V_{ds} = 5$ V and $V_{gs} = 0$ V.

some variation in detail from the analytic results of Section III and the resistive load unilateral results in Fig. 4, but are in good overall agreement.

V. Experimental Results

Experiments were performed on a commercial *C*-band, medium power packaged FET (MSC 88001), not specifically designed for doubler operation, in a 4- to 8-GHz doubler circuit. The device is mounted in a microstrip jig between two triple slug tuners and adjacent bias-T's. Couplers with power meters measure the input incident, reflected, and output powers. Input low-pass and output high-pass filters were also included in the test circuit. The output frequencies were monitored by means of a spectrum analyzer which also provided an approximate measure of the output power.

The package parasitics in this device cause the gate and drain ports to become series resonant at around 6 GHz. Thus, comparisons of the experimental results with theory are at best approximate. The experimental results are also taken with the circuit retuned for every input power level and gate bias change, and this is in contrast to simulation results which have fixed input and output circuits for any particular frequency. Results of experiments with fixed circuits show similar behavior to and good agreement with the simulation results of Fig. 5. At maximum doubler gain, the power-added efficiency was 8.2 percent.

Experimental results at higher frequencies show large conversion loss similar to those in Fig. 6, and have therefore not been included.

Conclusions

A simple analytic model has been used to estimate the contribution of the FET nonlinearities to doubler operation. The magnitude of doubler conversion gain and its frequency variation relative to the FET fundamental frequency gain are also estimated. Large signal computer simulations determine the limitations of the analytic model, and also provide a wider range of results. Experimental measurements on a 4- to 8-GHz doubler using a commercial FET show good agreement with theoretical predictions and simulation results.

This paper has shown that the largest contributor to the FET frequency doubler operation is the I_{ds} clipping effect. This suggests that the device is principally a resistive doubler and therefore harmonic conversion gain is expected to fall as $(1/n)^2$, where n is harmonic number.

Appendix

The characteristics of the FET in Fig. 2 are given by

$$I_{ds} = \left(1 - \frac{V_{gs}}{V_p}\right)^2 \left(I_{dss} + \frac{V_{ds}}{R_{do}}\right), \qquad \text{for } V_{ds} > V_{tan}$$

$$= \left(1 - \frac{V_{gs}}{V_p}\right)^2 \left\{I_{dss} + \frac{V_{ds}}{R_{do}} - I_{dss}\left(\frac{V_{tan} - V_{ds}}{V_{tan}}\right)^3\right\},$$

$$\text{for } V_{ds} < V_{tan}. \quad \text{(A.1)}$$

V_{tan} lies on the parabola passing through the origin, and the point (V_{dt}, I_{dt}), where

$$I_{dt} = \left(I_{dss} + \frac{V_{dt}}{R_{do}}\right). \quad \text{(A.2)}$$

It follows that

$$V_{tan} = V_{00}\left\{1 + \left(1 + \frac{2R_{do}I_{dss}}{V_{00}}\right)^{0.5}\right\} \quad \text{(A.3)}$$

where

$$V_{00} = \frac{\left(1 - \frac{V_{gs}}{V_p}\right)^2 V_{dt}^2}{2(I_{dss}R_{do} + V_{dt})}. \quad \text{(A.4)}$$

In the practical FET $V_{dt} \leq |V_p/2|$. From small signal *S*-parameter measurements R_{do} at $V_{gs} = 0$ V is determined.

and from this I_{dss} may be obtained from the value of I_{ds} at 0-V bias.

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Computer Calculation of Large-Signal GaAs FET Amplifier Characteristics

ANDRZEJ MATERKA AND TOMASZ KACPRZAK

Abstract—A simple and efficient method of GaAs FET amplifier analysis is presented. The FET is represented by its circuit-type nonlinear dynamic model taking into account the device's main nonlinear effects including gate–drain voltage breakdown. An identification procedure for extraction of the model parameters is described in detail and examples are given. The calculation of the amplifier response to a single-input harmonic signal is performed using the piecewise harmonic balance technique. As this technique is rather time-consuming in its original form, the optimization routine used to solve the network equations was replaced by the Newton–Raphson algorithm. Characteristics calculated with the use of the proposed method are compared with experimental data taken for a microwave amplifier using a 2SK273 GaAs FET unit. Good agreement at 9.5 GHz over wide ranges of bias voltage and input power levels are observed.

I. Introduction

THE GaAs FET is receiving continuously growing attention from circuit designers both in low-noise and high-power applications. Particularly, the power FET is an attractive device for use in microwave amplifiers and oscillators with its efficiency and power performance comparable or even superior to the other commercial solid-state or TWT sources. On the other hand, the power FET has received much less attention from researchers than its low-noise counterpart and, still, there is a need for data on device RF characterization at large-signal drive levels.

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Some efforts have been made to simulate the large-signal GaAs MESFET performance based on the numerical solution of the two-dimensional nonlinear differential equations describing the electron transport in the channel. The numerical results [1] are very helpful to understand device operation, but long computational time makes this approach impractical in circuit analysis and design programs. Recently, Madjar and Rosenbaum [2], [3] and Shur and Eastman [4] developed approximate analytical theories to model the active region under the gate of the microwave GaAs FET. Although one of these theories has been applied to the analysis of a practical microwave FET oscillator [3], both of them are of limited use in circuit design practice because they utilize the FET physical parameters which are scarcely available to the circuit designers. Willing, Rauscher, and de Santis [5] characterized an actual device with a quasi-static approach by measuring small-signal scattering parameters at a number of operating points to formulate an equivalent circuit, some of whose elements are bias-dependent. They use polynomial forms to approximate these dependences and a time-domain analysis program to calculate the large-signal device characteristics. The results obtained compare favorably with the experimentally determined characteristics, but the complexity of the equivalent circuit makes the identification technique of the model parameters rather laborious. Later, Rauscher [6]

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proposed an FET macromodel with a "lumped" nonlinearity, making it possible to analytically determine the optimum large-signal operating conditions of the FET in an oscillator circuit. A drawback of this approach is that the calculated optimum corresponds to a given combination of bias voltages. To achieve the circuit optimization over the entire range of the gate and drain voltages, one should perform a large number of measurements at elevated drive levels.

An alternative approach to the large-signal characterization of the microwave GaAs FET was used in the work of Tajima *et al.* [7]. They postulate that the large-signal device properties are governed primarily by the transistor dc characteristics—an assumption which has been verified at least up to 10 GHz. The Tajima model does not represent, however, the voltage-breakdown phenomenon [8] in the gate–drain region which is believed to have an impact on the FET gain saturation characteristics [9]. In order to take full advantage of the power capabilities of GaAs MESFET's, the breakdown effect is taken into account in the circuit-type large-signal dynamic model proposed in this paper.

The general problem of the microwave FET amplifier analysis is to derive a systematic procedure for defining the optimum input power, bias conditions, and terminating impedances that correspond to the maximum efficiency or output power at a given frequency. This can be facilitated greatly with the use of a computer and an appropriate large-signal analysis program. The computational task is to find a periodic steady-state response of a nonlinear network (i.e., the FET and its embedding circuit) to a single-input harmonic signal. The general-purpose time-domain analysis programs are not suitable for this aim because they are very time-consuming when applied to microwave circuits which typically consist of linear elements with a relatively small number of nonlinear ones. Additional difficulty arises from the fact that the time-delay effects as, e.g., the time difference between the changes in gate voltage and the relevant changes in the drain–source conduction current in the MESFET device, cannot be easily simulated with most time-domain analysis programs [10]. Another analysis method, of the simple iteration type, was applied by Tajima *et al.* [7] to the FET amplifier and oscillator design but sometimes it fails to converge, especially at high-input levels [11]. It follows then that the most efficient methods of proven value in the steady-state large-signal analysis of nonlinear circuits are the so-called piecewise harmonic balance techniques [12]. The network analyzed by these methods is decomposed into a minimum number of linear and nonlinear subnetworks and only frequency domain solutions of the linear subnetworks are required. In the original work of Nakhla and Vlach [12], an optimization procedure was used to solve the networks equations; however, it appears to be time-consuming and exhibits convergence problems at the high number of variables in the optimization process [13]. Taking the above considerations into account, the harmonic balance technique together with the Newton–Raphson method and appropriately formulated network equations [14] are used in the present work.

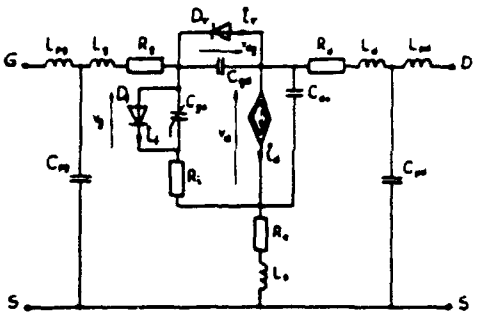

Fig. 1. FET large-signal equivalent circuit.

II. Large-Signal Dynamic GaAs MESFET Model

It was assumed, based on experimental study of arbitrarily selected transistors, that the main nonlinear elements of the model (see Fig. 1) are as follows [15]:

1) the equivalent gate-to-source capacitance C_{gs},
2) the diode D_f, which represents the current in the gate-to-channel junction,
3) the drain current source i_d controlled by voltage variables v_g and v_d,
4) the diode D_r, which represents the effect of the gate–drain breakdown. The diode parameters are not chosen to describe physical phenomena but to provide the best average fit to the experimental breakdown characteristics. The remaining parameters of this model are linear with their usual physical interpretation [16].

The nonlinear gate-to-source capacitance is given by

$$C_{gs} = C_{go}\left(1 - \frac{v_g}{V_{bi}}\right)^{-0.5}, \qquad \text{for } v_g < 0.8\,V_{bi} \tag{1}$$

and for $v_g \geq 0.8\,V_{bi}$ the plot of $C_{gs}(v_g)$ is approximated by a straight line with the slope equal to derivative dC_{gs}/dv_g obtained from (1) at $v_g = 0.8\,V_{bi}$. The parameters that appear in (1) are C_{go}, the gate-to-source capacitance for $v_g = 0$, and V_{bi}, the built-in potential of gate function.

The current of the diode D_f is given by

$$i_f = I_s\left[\exp(\alpha_s v_g) - 1\right] \tag{2}$$

with the model parameters I_s and α_s.

The voltage-controlled current source i_d is described by the formulas [17]

$$i_d = I_{dss}\left(1 - \frac{v_g}{V_p}\right)^2 \tanh\left(\frac{\alpha v_d}{v_g - V_p}\right) \tag{3}$$

$$V_p = V_{po} + \gamma v_d \tag{4}$$

where I_{dss}, V_{po}, α, and γ are the model parameters. In order to take into account the time delay between drain current and gate voltage, the instantaneous current $i_d(t)$ is calculated from (3) with $v_g = v_g(t - \tau)$ and $v_d = v_d(t)$, where τ is the model parameter.

The gate–drain breakdown effect is modeled by means of the diode D_r. The validity of such an approach was deduced from results of the two-dimensional computer simulation [18] and from dc breakdown characteristics measured for the transistors of various types, e.g., 2N6680 and 2SK273. The current in the diode D_r is given by

$$i_r = I_{sr}\left[\exp(\alpha_{sr} v_{dg}) - 1\right] \tag{5}$$

where I_{sr} and α_{sr} are the model parameters. It should be emphasized that the diode D_r does not represent any forward-biased p-n or Schottky-barrier junction connected between the gate and drain terminals. Instead, the current in the diode D_r approximates the breakdown current. For this reason, the parameters I_{sr} and α_{sr} in (5) are quite different in their values from the corresponding parameters I_s and α_s in (2). As a consequence, for small and moderate gate–drain voltages (e.g., up to 5 V for low-power FET's) and negative gate–source voltages, the gate current as calculated from (5) is negligibly small. However, it increases considerably at larger gate–drain voltages.

III. Determination of the Model Parameters

The model is characterized by a set of 24 parameters. Some of them are calculated from simple dc measurements, while others are fitted to dc and ac characteristics.

The parasitic source and drain resistances R_s and R_d can be determined by dc current and voltage measurements. R_s is found by passing a forward current I_G into the gate-source junction and measuring the resulting voltage at the floating drain with respect to the source [19]

$$R_s = \frac{\Delta V_{DS}}{\Delta I_G} \tag{6}$$

where ΔV_{DS} and ΔI_G are the incremental values of drain-source voltage and gate current, respectively. As the resistance R_s depends slightly on the gate current I_G, the average value obtained over a wide range of current can be used. Similarly, resistance R_d is found by forward biasing the gate–drain junction and measuring the voltage at the floating source.

The gate resistance R_g can be estimated from the measured I–V characteristic of the gate-source real Schottky diode

$$V_{GS} = I_G R + \frac{1}{\alpha_s} \ln \frac{I_G}{I_s} \tag{7}$$

where R is the series diode resistance and I_s, α_s are the parameters of (2). When $I_G R \ll \alpha_s^{-1} \ln(I_G/I_s)$, i.e., for low forward current I_G, the V_{GS} can be approximated by a second term on the right side of (7). The parameters I_s and α_s can then be obtained from the linear portion of the plot $\ln I_G$ versus V_{GS}. Substituting the values of I_s and α_s into (7), one can find the value of R from the $I_G - V_{GS}$ plot at high gate currents. Next, the gate-metalization resistance R_g is estimated as in [19]

$$R_g = \frac{R - R_s}{3}. \tag{8}$$

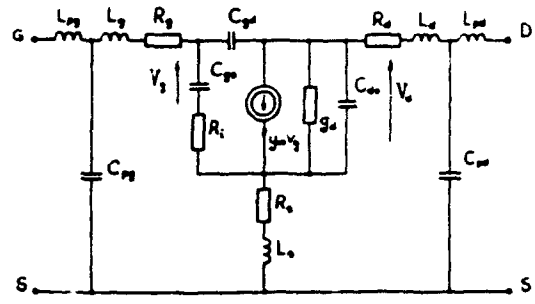

Fig. 2. FET small-signal equivalent circuit.

It was found from measurements that for gate-source voltage range $V_{GS} < V_p$ (the channel is pinched off regardless of drain-source voltage) the gate-drain breakdown current increases exponentially with increasing drain bias, and the breakdown characteristic does not depend on the voltage V_{GS}. Plotting $\ln i_r$ versus gate–drain voltage V_{DG}, one can obtain the parameters α_{sr} and I_{sr}.

The parameters I_{dss}, V_{po}, α, and γ are computer optimized to fit the dc $I_D - V_{DS}$ characteristics calculated from (3) and (4) to the measured ones in the triode and pentode regions, from zero up to breakdown voltage. Knowing the values of R_s and R_d, the internal voltages v_g and v_d can be calculated for each pair of external voltages V_{GS} and V_{DS} by means of the Newton–Raphson method—it needs about 3–4 iterations for a given accuracy of 1 μV. The maximum error of this global fitting did not exceed a few percent.

The remaining parameters of the FET model are determined using the small-signal equivalent circuit of the device shown in Fig. 2. The linear current source is described by the admittance

$$y_m = g_m \exp(-j\omega\tau) \tag{9}$$

where g_m is the transconductance at low frequencies. At the given quiescent operating point, the values of the transconductance g_m and the output conductance g_d are calculated as the drain current derivatives with respect to the gate-source voltage and drain-source voltage, respectively, with the drain current described by (3). Next, using these values of g_m and g_d together with the previously obtained values of R_s, R_d, and R_g, the remaining model parameters can be obtained by means of the computer fitting of the calculated S-parameters to the measured data in a prescribed frequency range [20].

The set of MESFET model parameters determined for a Mitsubishi 2SK273 unit (maximum total power dissipation at 25°C ambient, $P_T = 300$ mW) using the identification procedure as described above is given in Table I. The S-parameters were measured in the frequency range of 2–10 GHz at the bias voltages of $V_{GS} = -0.75$ V and $V_{DS} = 4$ V, which correspond nearly to the maximum power-added efficiency. The value of built-in voltage V_{bi} was assumed equal to 0.8 V. Fig. 3(a) shows the measured dc $I_D - V_{DS}$ output characteristics of the FET used for extraction of the model parameters I_{dss}, V_{po}, α, and γ, while in Fig. 3(b) are shown the calculated characteristics

TABLE I
MODEL PARAMETERS FOR A 2SK273 MESFET DEVICE

R_s [ohm]	4.5	I_{dss} [mA]	75.0	L_s [nH]	0.1
R_d [ohm]	4.5	V_{po} [V]	-1.78	L_d [nH]	0.2
R_g [ohm]	4.5	α [-]	3.35	L_g [nH]	0.2
R_i [ohm]	10.0	δ [-]	-0.11	τ [ps]	5.0
α_s [V^{-1}]	23.0	C_{go} [pF]	0.64	C_{pg} [pF]	0.26
I_s [nA]	1.05	V_{bi} [V]	0.80	C_{pd} [pF]	0.20
α_{sr} [V^{-1}]	1.28	C_{dg} [fF]	26.0	L_{pg} [nH]	0.67
I_{sr} [nA]	6.50	C_{ds} [pF]	0.10	L_{pd} [nH]	0.61

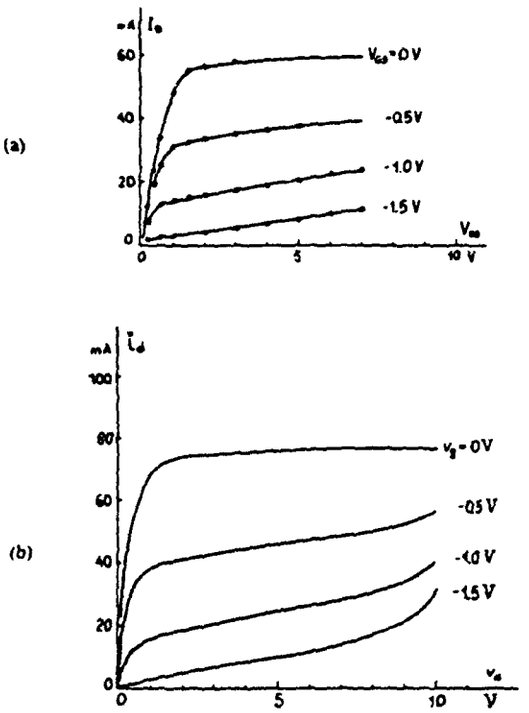

Fig. 3. (a) Measured (OOO) and calculated (——) dc characteristics of a 2SK273 unit. (b) Calculated characteristics of the internal transistor, including breakdown effects.

of the internal transistor including the voltage-breakdown effect.

IV. FET Amplifier Analysis

A simplified block diagram of the FET amplifier under consideration is shown in Fig. 4(a) where $Z_o = 50\ \Omega$, typically. One of the most important characteristics of the FET, which describes the power-handling capability of the device at a given frequency, is the dependency of the power delivered to the load P_o on the input power P_i. This is the so-called gain-saturation characteristic (often used in practical design procedures [6], [21]) which is measured with the input and output tuners adjusted for maximum P_o at a

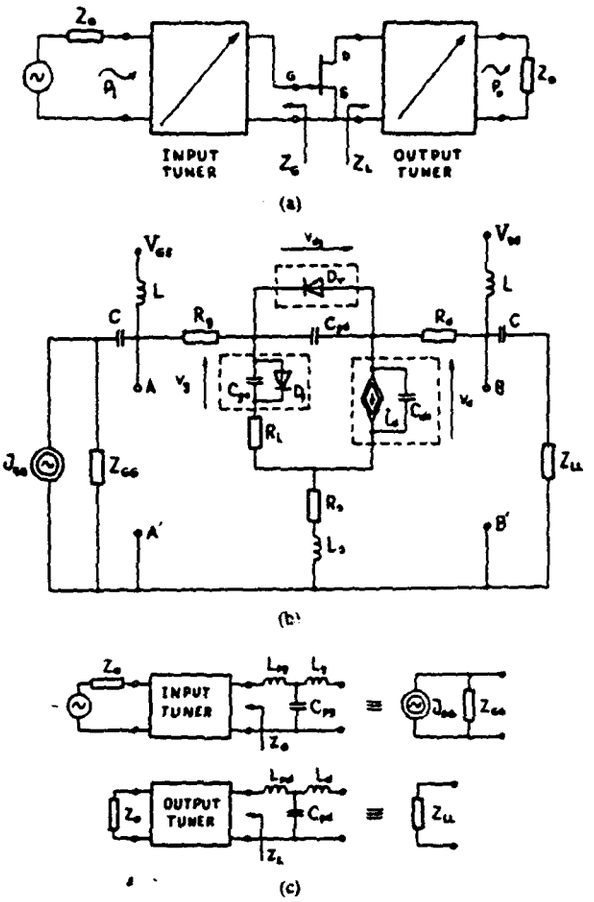

Fig. 4. (a) Simplified block diagram of an FET amplifier. (b) Large-signal equivalent circuit of the amplifier. (c) Equivalent transistor terminating circuits.

given P_i. To simulate this with the digital computer, the MESFET model proposed in this paper was used. After combining these linear and lossless elements of the model that represent gate and drain parasitics with the impedances Z_G and Z_L seen at the transistor terminals (see Fig. 4(a)) one obtains a simplified equivalent circuit of the amplifier as shown in Fig. 4(b). Dummy elements L and C in Fig. 4(b) represent, respectively, an open and short circuit at the signal frequency. V_{GS} and V_{DS} are the bias voltages, Z_{GG} and Z_{LL} are, respectively, the equivalent input and output terminating impedances. Their values can be easily calculated once the FET parasitics and the impedances Z_G and Z_L are measured (see Fig. 4(c)). J_{GG} stands for the input signal equivalent source.

For given values of frequency, J_{GG}, Z_{GG}, and Z_{LL}, one can calculate the response of the circuit of Fig. 4(b) using the harmonic balance technique. For its implementation, three nonlinear subnetworks were extracted from the amplifier equivalent circuit. These are shown inside the dashed boxes in Fig. 4(b). The Fourier coefficients of $v_g(t)$ and $v_d(t)$ have been chosen as independent variables in the harmonic balance routine [14]. The voltage $v_{dg}(t)$

was expressed in terms of v_g and v_d using Ohm's and Kirchhoff's laws.

Having the fundamental components of v_g and v_d one can calculate the input power at the terminals $A-A'$ (see Fig. 4(b)) and the output power at $B-B'$. Since the tuners' circuits and FET parasitics have been assumed lossless, these powers are equal to P_i and P_o, respectively. In order to calculate the power gain saturation characteristics, an optimization procedure was employed to find, for every given value of P_i, the values of Z_{GG} and Z_{LL} that correspond to the maximum of P_o. An objective function was defined as

$$E = \text{abs}(P_i - P_i^x) + \text{abs}(K - P_o^x) \qquad (10)$$

where P_i is the power available from the signal source, P_i^x is the actual power delivered to the amplifier input, K is a constant higher than any expected output power level, and P_o^x is the actual power delivered to the load. Obviously, the quantities P_i^x and P_o^x in (10) depend on the terminating impedances and the objective function has its minimum that corresponds to the impedances that match simultaneously both the input and output ports of the FET. A program was written to calculate the power gain saturation characteristics using the HP 9825A desk computer. A modified Davies–Swann–Campey direct-search minimization procedure [13] and the modified harmonic balance technique [14] were implemented in the program which occupies about 15k bytes of the computer memory.

V. Results

To calculate the power gain characteristics of the 2SK273 FET unit, the model parameters already specified in Section III are used. The parameters have been determined from the static I-V characteristics and from the small-signal S-parameters measured at the frequencies up to 10 GHz. On the other hand, the input signal frequency is chosen $f = 9.5$ GHz in the present example. Then, the model validity is not checked at the harmonic frequencies. Therefore, in the final analysis, only the dc component and the fundamental harmonic were used. However, this simplification does not generate a significant error, at least when the large-signal characteristics of an FET tuned amplifier are concerned, as can be seen later. The Newton–Raphson algorithm combined with the harmonic balance method [14] requires 4–10 iterations to calculate the amplifier voltage response with an error less than 1 mV, depending on the input power level. It takes about 10 min of the HP 9825A computer time to find values of Z_{GG} and Z_{LL} that match the simulated amplifier at a given value of P_i.

In Fig. 5 are shown the calculated power saturation characteristics obtained for the impedances Z_{GG} and Z_{LL} matching the transistor at every given input power P_i. The calculations were performed for $V_{DS} = 4$ V and two values of gate-source voltage: $V_{GS} = -0.75$ V and $V_{GS} = -1.25$ V. For input power $P_i \geq 5$ mW, the decrease in the transistor power gain is accompanied by a dc gate current flow, as it is seen in Fig. 5. This current consists of two components.

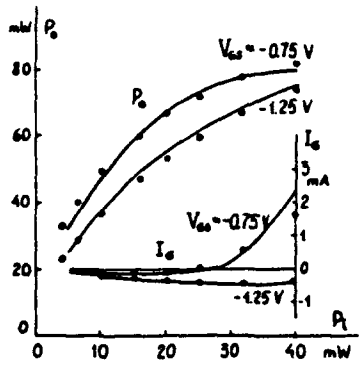

Fig. 5. Output power P_o and dc gate current I_G versus input power P_i. Measurements (OOO), calculations (——), $f = 9.5$ GHz, and $V_{DS} = 4$ V.

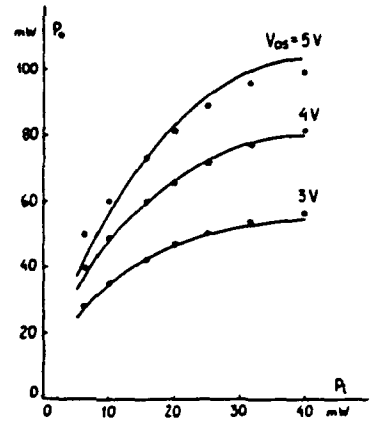

Fig. 6. Measured (OOO) and predicted (——) power-saturated characteristics, $f = 9.5$ GHz and $V_{GS} = -0.75$ V.

The negative component represents the breakdown effect while the positive one is due to the forward conduction of the gate junction [22]. In the case of $V_{GS} = -0.75$ V and small input power levels, the breakdown current dominates the forward conduction component, while for larger powers ($P_i \geq 30$ mW) the forward conduction is prevailing. In the case of $V_{GS} = -1.25$ V, in the whole range of input power up to 40 mW, the dc gate current is negative. Also shown in Fig. 5 are the results of measurements obtained using a load-pull technique [23]. Good agreement between theory and experiment is observed for the FET bias conditions as described previously.

In Fig. 6 are shown the power saturation characteristics for $V_{GS} = -0.75$ V and three values of drain-source voltage $V_{DS} = 3$, $V_{DS} = 4$, and $V_{DS} = 5$ V. Some discrepancies between the calculated and measured data are observed for $V_{DS} = 5$ V. These are attributed to the simplified description of the breakdown phenomena in the FET model. Particularly, the dynamics of the breakdown mechanisms [24] must be included in the GaAs FET model. The mathematical model (5) is of an instantaneous nature, but in general the breakdown effects may have time delays associated with them.

For every given value of P_i there exists a set of FET terminating impedances that corresponds to a maximum

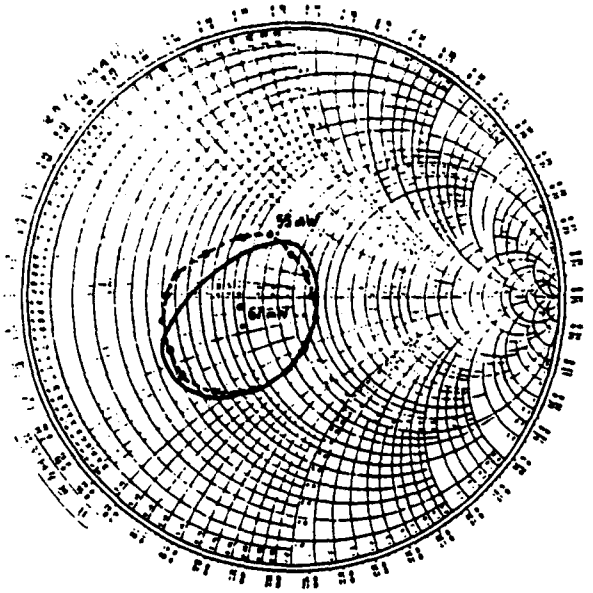

Fig. 7. Measured (OOO) and predicted (——) contours of constant output power on the load impedance plane, $Z_L/50\ \Omega$, $f = 9.5$ GHz, $V_{DS} = 4$ V, $V_{GS} = -0.75$ V, and $P_i = 20$ mW.

output power. Putting K in (10) less than this maximum value, one can calculate constant output power contours on the terminating impedances planes. These contours indicate how the output power of the FET varies as the function of the load impedance presented to it (see Fig. 4(a)). This information is very useful in designing practical amplifier and oscillator circuits. Measured and predicted contours of constant output power of the FET amplifier under consideration are shown in Fig. 7, for $P_i = 20$ mW, $V_{DS} = 4$ V, $V_{GS} = 0.75$ V, and the impedance Z_G (Fig. 4(a)) matching the amplifier's input. Considering the limited accuracy of impedance measurements at microwave frequencies, the agreement is very good.

VI. Conclusions

The reasonably simple and fairly accurate large-signal dynamic circuit-type model for a GaAs MESFET that is appropriate for use in circuit design programs has been proposed. The identification procedure of the model parameters is based on the experimental characterization of the FET dc current-voltage relationship and the frequency dependent small-signal S-parameters. The computer analysis of a large-signal X-band FET amplifier and the measurements of its performance have confirmed the validity of the model, in which only four elements were assumed to be nonlinear, i.e., C_{gs}, D_r, D_f, and i_d (see Fig. 1). These elements predominantly represent the power gain saturation of the transistor.

The model has been used to calculate the large-signal FET characteristics in the amplifier circuit with the use of a digital computer. The amplifier analysis method is based on the piecewise harmonic balance technique [12] with the originally recommended optimization procedure replaced by the Newton–Raphson computational scheme [14]. This modification considerably shortens the calculation time and enables us to perform an analysis and design process on the desk computer. Since nonlinear device operations as either power amplifiers and oscillators is quite similar, the FET characterization technique developed above for amplifiers can be readily carried over to meet oscillator design needs as well.

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Dr. Kacprzak is a member of the Polish Society of Theoretical and Applied Electrical Science (PTETIS).

A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers

WALTER R. CURTICE, SENIOR MEMBER, IEEE, AND M. ETTENBERG, LIFE SENIOR MEMBER, IEEE

Abstract—A nonlinear equivalent circuit model for the GaAs FET has been developed based upon the small-signal device model and separate current measurements, including drain-gate avalanche current data. The harmonic-balance technique is used to develop the FET RF load-pull characteristics in an amplifier configuration under large-signal operation. Computed and experimental load-pull results show good agreement.

I. Introduction

THE GENERAL-PURPOSE nonlinear circuit analysis programs that exist were designed primarily for transient (time-domain) analysis of silicon integrated circuits [1], [2]. By adding new models for GaAs devices, Curtice [3] and Sussman-Fort *et al.* [4] show that these programs can be used for the study of GaAs integrated circuits. However, a more sophisticated model is required to study GaAs power FET's operated at high dc-to-RF conversion efficiency. Such a model must contain an accurate description of all important device nonlinearities and also efficiently analyze the external microwave circuit interaction over many RF cycles. The circuit reactances lead to time constants large relative to the RF period. Time-domain analysis is thus inefficient and, in fact, unnecessary since the reactances are linear.

Rizzoli *et al.* [5] described a general-purpose nonlinear microwave circuit design technique that efficiently analyzes the device–circuit interaction by application of the "harmonic-balance" technique [6]. Camacho-Penalosa [7] described the application of this technique to the microwave FET.

In GaAs power amplifiers, the load-pull method is often used to experimentally obtain optimum load conditions at large-signal operation [8]. Sechi [9] developed a graphical extension of this technique to maximize the RF power output subject to a specified maximum value of intermodulation distortion. However, the load-pull measurements are time consuming and difficult at high RF frequencies. An analytical technique would be very advantageous.

Tajima and Miller [10], Willing *et al.* [11], Peterson *et al.* [12], and others have reported nonlinear GaAs FET models for the design of power amplifiers. We have extended the work of Peterson *et al.* and made detailed comparisons of computed and measured load-pull characteristics using a nonlinear analysis program for the GaAs FET amplifier based upon the harmonic balance technique.

Materka and Kacprzak [13] recently proposed a large-signal analysis of a GaAs FET amplifier. Our model is similar but has significant differences in detail. We measure avalanche breakdown voltage for devices and use these values in the analytical model. The nonlinear gate-to-source capacitance variation that we measure is different from the ideal variation assumed by Materka and Kacprzak. We also include second- and third-harmonic voltages in the analysis and show this to be significant. Nevertheless, the agreement shown by Materka and Kacpzak between their measurements and model calculations is excellent.

Our nonlinear device model has evolved from the self-consistent GaAs FET small-signal model reported by Curtice and Camisa [14]. This program provides a computer-aided means to develop output circuit designs that optimize the amplifier performance (i.e., efficiency, bandwidth, etc.). Accurate prediction of large-signal load-pull performance is essential to accurately design output networks. In addition, we operate the program on Hewlett-Packard 1000 RTE minicomputers to reduce the cost of computation.

Section II reviews the nonlinear analysis program. The FET model and the method of evaluation of the nonlinearities are presented in Section III. Mathematical equations are presented in Section IV. The remaining sections describe analytically generated load-pull results and their comparison with measured load-pull data. Large-signal FET simulations by the nonlinear program are also compared with simulations from a two-dimensional device model. This comparison shows the importance of including the third harmonic of voltage in the output circuit.

II. The Nonlinear FET Program

This program consists of a time-domain model of the GaAs MESFET coupled with frequency-domain models for the input and output matching circuits. The nonlinear FET elements must be analyzed in the time domain to preserve their physical nature. The linear circuit response to the FET current excitation can be analyzed in the frequency domain by standard techniques. Transformation

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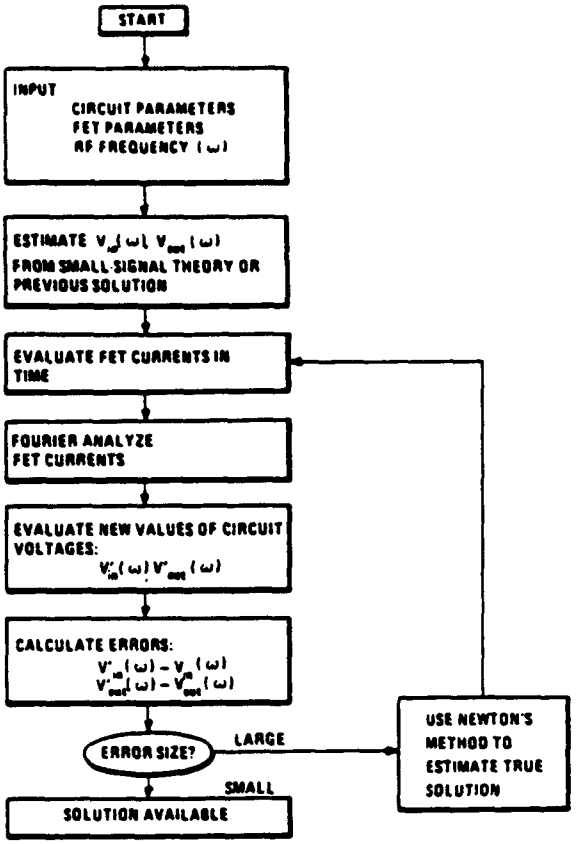


Fig. 1. Program flow chart.

between the time and the frequency domains is accomplished using a discrete Fourier transform. A valid physical solution is obtained when the voltage waveform at the input (or output) of the FET produces a current waveform into the device that is the negative of that into the RF circuit to within some small error. The program flow chart is shown in Fig. 1. The method of successive approximation is used with less than 100-percent update to assure convergence.

III. Evaluation GaAs MESFET Nonlinearities

Fig. 2 shows the equivalent circuit model assumed. This model is noticeably different than used by Curtice and Camisa for accurate small-signal modeling of GaAs MESFET's. The drain-channel capacitor is omitted to simplify node current equations. This produces some loss of accuracy. In addition, two new current sources are used. The drain-gate voltage-controlled current source represents the drain-gate avalanche current that can occur at large-signal operation. The gate-source voltage-controlled current source represents gate current that occurs when the gate-source junction is forward biased. The third current source $I_{ds}(V_{in}, V_{out})$ is the large-signal form of the usual small-signal transconductance.

Fig. 3 shows the measured dc current-voltage relationship for an RCA device studied. This data is measured in the automated Fukui [15] equipment, and Kelvin probes are used (and required) to obtain accurate data. Fig. 4 shows data on the same device for larger drain-source voltages. The data for higher currents in Fig. 3 are appreciably influenced by heating effects. However, this should not cause large error in the nonlinear model. Fig.. 4 shows that the device pinchoff voltage increases appreciably at larger drain-source voltage. The early version of the nonlinear program assumed a square-law relationship between the (saturation) current and the gate-source voltage. Real devices often do not exhibit such a relationship and it is more accurate to use a cubic approximation

$$I_{ds} = \left(A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3\right) \cdot \tanh\left(\gamma \cdot V_{out}(t)\right)$$

where V_1 is the input voltage. The coefficients A_i can be evaluated from data in the saturation region at the same time the data of Fig. 12 is measured. We use a simple Fortran program for evaluation of the A_i's with least-square error. One disadvantage of the cubic relationship is that unlike the quadradic, a pinchoff voltage may result that makes current zero or transconductance zero, but not both.

The following method is used to include the phenomenon of pinchoff voltage increase with drain-source voltage (Fig. 4). We assume

$$V_1 = V_{in}(t - \tau) \cdot \left[1 + \beta\left(V_{out}^0 - V_{out}(t)\right)\right]$$

where

- β coefficient for pinchoff change,
- V_{out}^0 output voltage at which A_0, A_1, A_2, A_3 were evaluated, and
- τ internal time delay of FET.

The form of this equation is not physically significant. Measured RF data (see Appendix A) shows that τ is a direct function of drain-source voltage, or

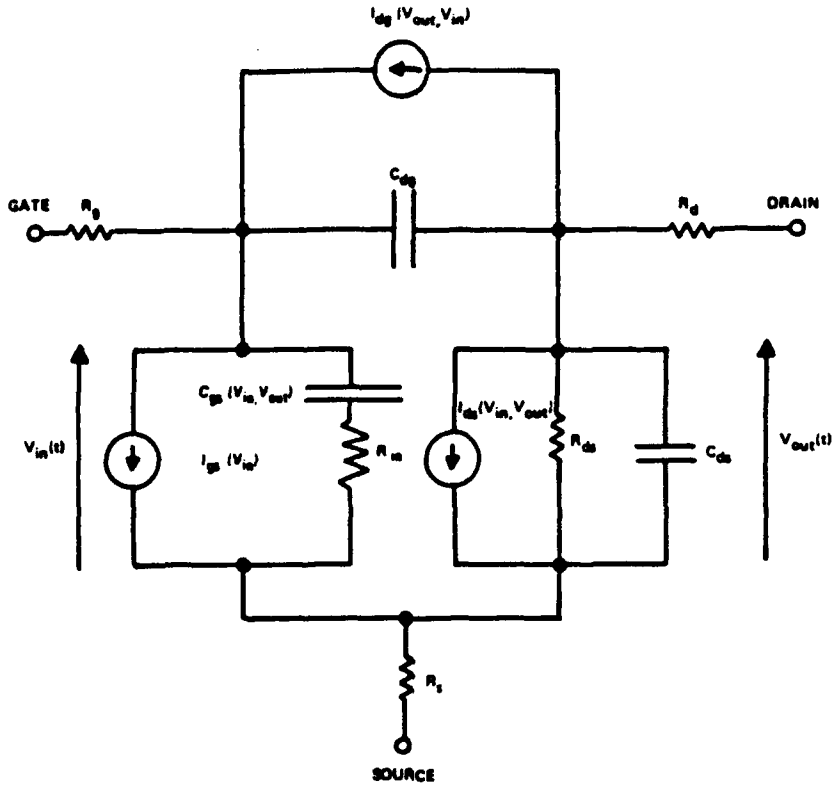
$$\tau = A_5 \cdot V_{out}(t).$$

Fig. 5 shows the current-voltage relationship calculated using these equations for the RCA device whose characteristics were shown in Figs. 3 and 4. This technique produces an accurate approximation to the measured data.

Pulsed measurement of drain-gate avalanche currents were made on a number of devices. Fig. 6 shows data for the device previously studied (Figs. 3 and 4). Notice that the drain currents cannot be pinched off at large drain-source voltages due to the gate current produced by avalanche breakdown. This is an important phenomenon that limits both RF current and power output. In this model, the drain-gate avalanche current is taken to be

$$I_{dg} = \begin{cases} \dfrac{V_{dg}(t) - V_B}{R_1}, & V_{dg} > V_B \\ 0, & V_{dg} < V_B \end{cases}$$

where $V_B = V_{B0} + R_2 \cdot I_{ds}$, R_1 is the approximate breakdown resistance, and R_2 is the resistance relating breakdown voltage to channel currents.



EQUIVALENT CIRCUIT OF GaAs MESFET

Fig. 2. Equivalent circuit model of the GaAs MESFET.

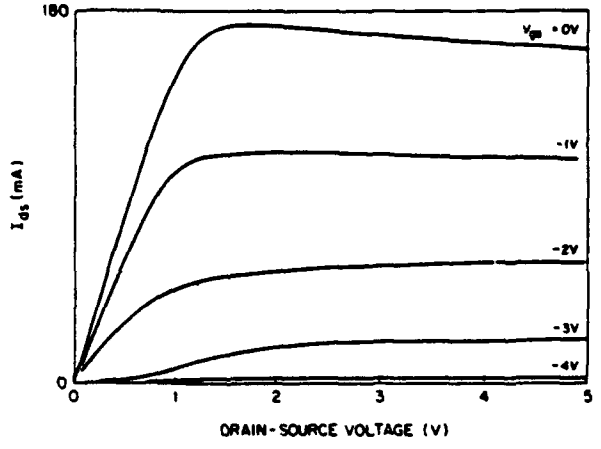


Fig. 3. Measured current–voltage relationship for RCA device B1512-3A.

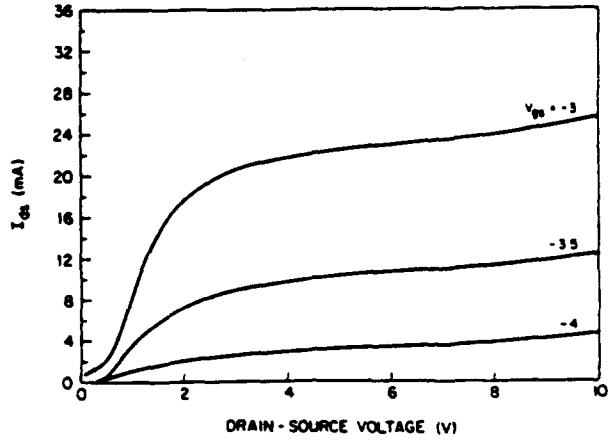


Fig. 4. Same as Fig. 12 but for larger drain-source voltages.

The forward-biased gate current is taken to be

$$I_{gs} = \begin{cases} \dfrac{V_{in}(t) - V_{bi}}{R_F}, & V_{in}(t) \geq V_{bi} \\ 0, & V_{in}(t) < V_{bi} \end{cases}$$

where V_{bi} is the built-in voltage and R_F is the effective value of forward-bias resistance.

The values of R_g, R_d, and R_s are obtained from the automated Fukui measurements. The values of C_{dg}, C_{gs}, R_{ds}, and C_{ds} at the bias point are obtained from the small-signal model using the technique developed by Curtice and Camisa. Although both C_{gs} and C_{dg} are nonlinear functions of voltage, computation including these characteristics produced only small effects upon the RF saturation characteristics.

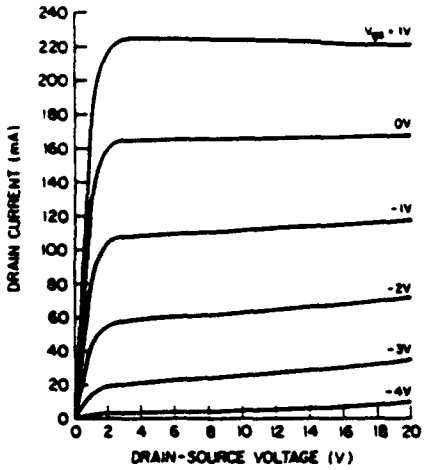


Fig. 5. Current–voltage relationships for RCA device B1512-3A as calculated by the analytical equations.

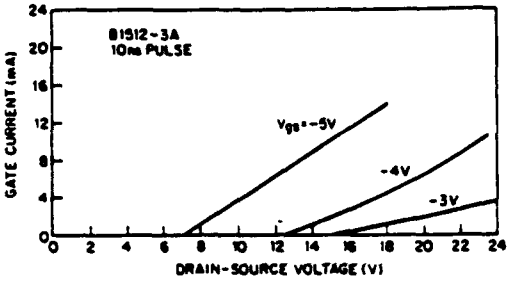


Fig. 6. Pulsed current–voltage data for RCA device B1512-3A.

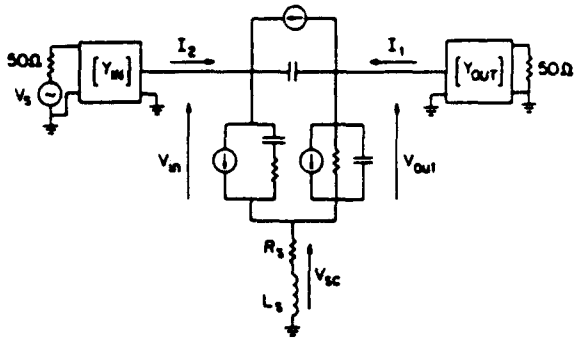


Fig. 7. Equivalent circuit model of GaAs MESFET amplifier as used in the nonlinear analysis program.

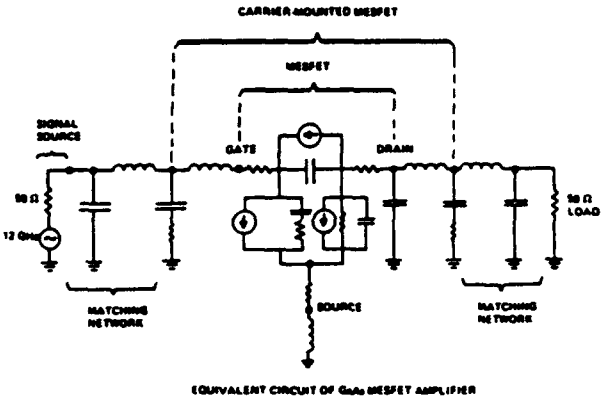


Fig. 8. Equivalent circuit model of GaAs MESFET amplifier showing specific topology for matching circuits.

The drain-source resistance is also a strong function of V_{gs} and V_{ds}. However, differentiation of the drain current in the model gives the following result for small-signal output RF conductance:

$$g_{ds} = \frac{1}{R_{ds}} - g_{m0}\beta V_{in} + \frac{\gamma I_{ds0}\cdot \operatorname{sech}^2\left[\gamma V_{out}(t)\right]}{\tanh\left(\gamma V_{out}(t)\right)}$$

where

$$g_{m0} = \left(A_1 + 2A_2V_1 + 3A_3V_1^2\right)\cdot\tanh\left[\gamma\cdot V_{out}(t)\right].$$

The three terms comprising g_{ds} may be understood to be: 1) a fixed conductance term; 2) a substrate conductance term that causes the pinchoff voltage change with V_{ds}; and 3) a channel conductance term that is important only at low drain-source voltages (i.e., below current saturation). The net result is that the output RF conductance depends upon V_{gs} and V_{ds} consistent with actual device behavior.

The small-signal intrinsic transconductance can similarly be evaluated by differentiation of drain current with respect to V_{in}. The result is

$$g_m = g_{m0}\left[1 + \beta\left(V_{out}^0 - V_{out}(t)\right)\right].$$

Coefficient β causes the transconductance to decrease with increasing drain-source voltage, consistent with the behavior of GaAs FET's.

In summary, the equivalent circuit model has been constructed with the simplified circuit shown in Fig. 2. The principal nonlinearities are the voltage-controlled current sources. These must be characterized for each device. It was found to be important to include the bias dependance of pinchoff voltage in the drain-current source. The small-signal properties of the model were found to be consistent with the FET behavior.

IV. Description of the Computer Program NFET

The program NFET was described briefly in Section II. We now describe the analysis of the FET amplifier using this program.

Fig. 7 shows the lumped-element equivalent circuit model of the GaAs MESFET amplifier. The two-port networks $[Y_{in}]$ and $[Y_{out}]$ are matching networks presumably designed for maximum power transfer at the input and the output, respectively. Notice that the gate and drain resistances of the FET are absorbed into these networks. Fig. 8 shows a typical topology for a carrier-mounted FET. The first design of these networks is usually done using SUPER-COMPACT™ [16] to achieve conjugate matching at input and output for small-signal operation. This produces the maximum gain condition. Once a trial design is available, the Y-transfer characteristics can be evaluated.

The input voltage is

$$V_{in}(t)+V_{ic}(t)=V_{gs}^{dc}+\sum_n\left[a_n\sin(n\omega t)+b_n\cos(n\omega t)\right]$$

where $V_{ic}(t)$ is the voltage drop across the source resistance and inductance which is assumed to be

$$V_{ic}(t)=V_{ic}^{dc}+\sum_n\left[c_n\sin(n\omega t)+d_n\cos(n\omega t)\right].$$

The output device voltage is

$$V_{out}(t)+V_{ic}(t)=V_{ds}^{dc}+\sum_n\left[f_n\sin(n\omega t)+g_n\cos(n\omega t)\right].$$

The present version of NFET uses dc, fundamental-, second-, and third-harmonic voltage components. The time-domain expressions for $V_{in}(t)$ and $V_{out}(t)$ are used to generate device currents. For example, the total drain current consists of drain-source current

$$I_{ds}\left[V_{in}(t),V_{out}(t)\right]+C_{ds}\frac{d}{dt}V_{out}(t)+\frac{V_{out}(t)-V_{out}^{dc}}{R_{ds}}$$

plus drain-gate displacement current

$$C_{dg}\frac{d}{dt}\left[V_{out}(t)-V_{in}(t)\right]$$

and the avalanche current if $[V_{out}(t)-V_{in}(t)]>$ the breakdown voltage V_B.

The drain and gate currents are then Fourier analyzed to find their frequency components using a discrete Fourier transform. Linear circuit elements, such as C_{dg}, need not be included since the answers are known *a priori*.

V. FET Load-Pull Simulation

As an application of the nonlinear analysis program (NFET), a load-pull program was written to simulate the FET performance at high drive levels under variable load conditions. The program runs interactively on the HP1000/A900 and plots contours of constant power output on a Smith Chart.

The algorithm which controls the load pull relies on the fact that the contours of constant power are closed curves and that the power within a given contour is higher than the contour power while the power outside is lower than the contour power. The load pull is designed to proceed in a counterclockwise direction from the first point designated as a contour point. A test point is taken by increasing the radius vector of the reflection coefficient to the given point. If the power at the test point is greater than the contour power, the test point rotates clockwise to find the next contour point. If the test point gives a lower power, then it is outside the contour and the test point is rotated counterclockwise to find the next contour point. The "width" of the contour is programmable and is usually taken as 1 percent of the contour power. If the calculated power points fall outside this limit, the algorithm interpolates between the two nearest values.

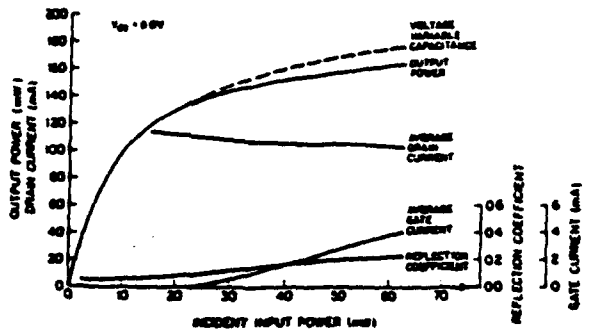


Fig. 9. Output RF power, average drain current, average gate current, and reflection coefficient as a function of RF input power for RCA device B1512-3A at 12 GHz with $V_{ds}=8$ V, $V_{gs}=-1$ V. The output is tuned for high gain.

VI. Comparison with Experimental Data

Fundamental- and second-harmonic voltages are used for the calculation presented in this section. Fig. 9 shows the calculated RF power output as a function of RF power input for RCA device B1512-3A for a case of output matching for high gain. Strong output power saturation occurs due to the large RF voltage amplitudes. As the degree of saturation increases with increase of RF input power, the computed average drain current decreases, the average gate current increases, and the reflection coefficient at the input increases as seen in Fig. 9. These effects are in agreement with experimental observations. These calculations were made assuming a constant value of gate-source capacitance. The dashed output power curve shows the result for voltage-variable gate-source capacitance. Here a square-root relationship was assumed with a built-in voltage of 1 V. This variation is much larger than measured but produces less than a 10-percent increase in the output power. Therefore, the assumption of a constant gate-source capacitance does not greatly effect the accuracy of the results. The reason for this behavior is described in Appendix B.

By reducing the shunt resistive loading of the output circuit, higher RF power output can be achieved. Fig. 10 shows the input/output power relationship calculated at two different output loadings. The case of lower shunt impedance (73 Ω) is very similar to the measured data (also plotted in Fig. 10). However, there is more gain and more (forward-biased) gate current in the calculated results. This indicates that the model does not fully reproduce the operating conditions.

The power data of Fig. 10 are replotted in Fig. 11 using a logarithmic scale. Note that there is about 2-dB difference in the power gain for the data and the lower shunt impedance case. A portion of the 2 dB is believed to be due to input losses in the tuner used in the measurements.

Load-pull contours are developed as follows: The load is adjusted for maximum output power for a given RF drive power. Then the load is changed to produce less output power (e.g., −1 dB), and a load contour for constant power is measured.

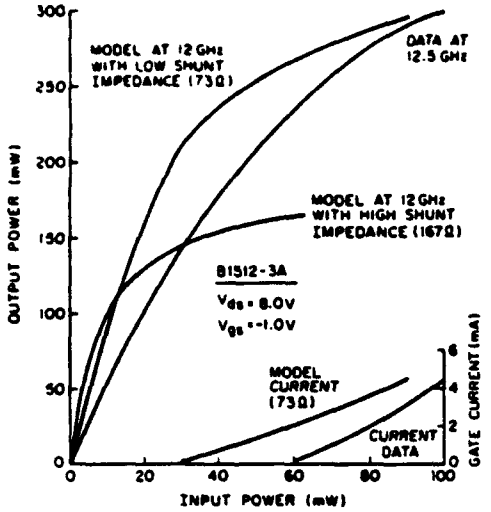


Fig. 10. RF power output as a function of RF power input for device B1512-3A with $V_{ds} = 8$ V, $V_{gs} = -1$ V. The curves starting at origin are calculated at 12 GHz and the third curve is measured data at 12.5 GHz.

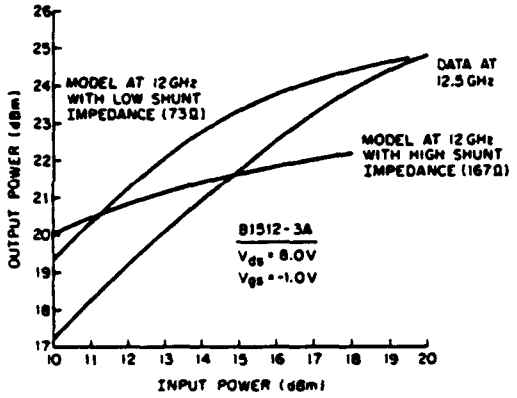


Fig. 11. Measured and calculated RF power output as a function of RF power input for device B1512-3A with $V_{ds} = 8$ V, $V_{gs} = -1$ V, and plotted on a logarithmic scale.

Fig. 12 shows the calculated and measured load-pull contours (for a nominal maximum output power of 200 mW) for this device for 176- and 145-mW power output at 12 GHz. The agreement is good. Fig. 13 shows the calculated and measured points of the load for maximum power output for various output power values. These do not agree as well as seen in other devices.

Fig. 14 shows the effect of harmonic voltages upon the input/output power calculated for this device with optimized output loading. Note that neglecting the second harmonic significantly changes the output power in the saturation region. However, it is difficult to evaluate accurately the impedance seen at each harmonic in a given circuit. The impedance used for this calculation assumes lumped-element matching.

Fig. 15 shows the calculated load-pull contour for 175-mW output power for a second RCA device at 50-mW RF input power. However, in the experiment, the RF input

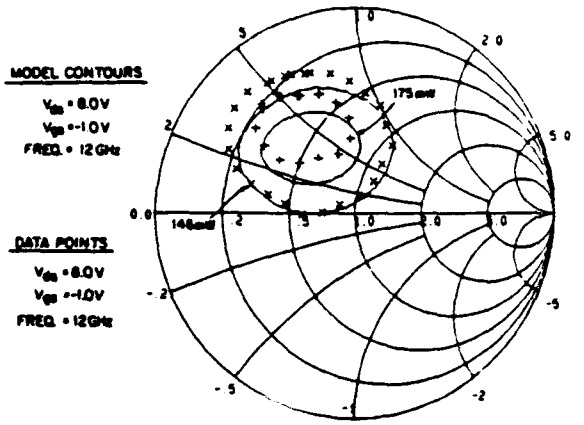


Fig. 12. Smith Chart display of calculated and measured load-pull contours for device B1512-3A at 12 GHz.

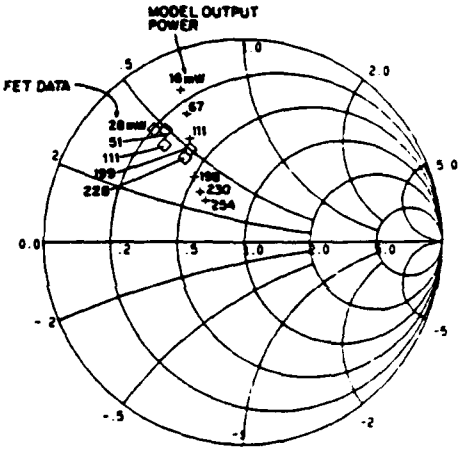


Fig. 13. Smith Chart display of calculated and measured optimum RF output loads for device B1512-3A at 12 GHz.

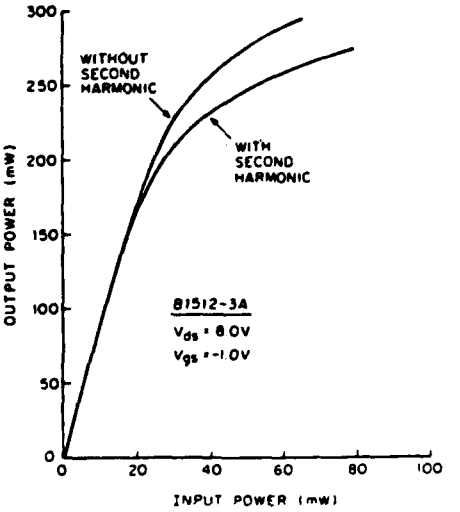


Fig. 14. RF output versus input calculated with and without second-harmonic voltages for device B1512-3A at 12 GHz.

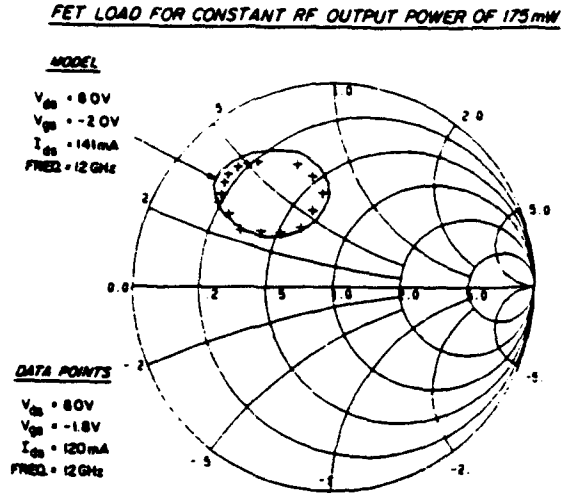


Fig. 15. Smith Chart display of calculated and measured RF output loads for constant output power of 175 mW for device B1824-1C at 12 GHz.

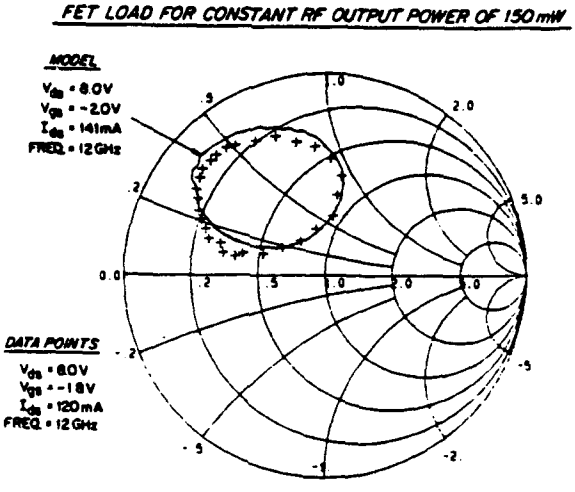


Fig. 16. Smith Chart display of calculated and measured RF output loads for constant output power of 150 mW for device B1824-1C at 12 GHz.

power was 104 mW. Fig. 16 shows the same comparison for an output power of 150 mW with the same drive conditions. There is good agreement with regard to output load-pull characteristics for a given output power, but disagreement in driver power (and gain) by approximately 3 dB. Some of this error is attributable to losses in the input tuner used in the measurements, although the actual value of tuner loss was not measured.

The maximum RF power output for the simulation with 50-mW input power is 216 mW. In the experiment using a 104-mW RF drive, the maximum RF power output was 205 mW.

Fig. 17 shows the load conditions for maximum power output at seven different output power values as computed by the nonlinear program. Measured data are also shown and are in good agreement.

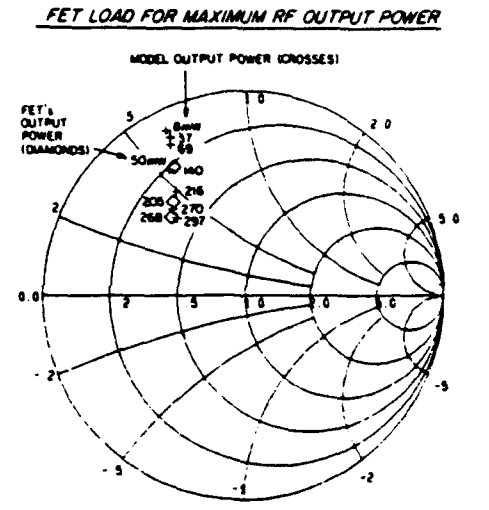


Fig. 17. Smith Chart display of calculated and measured optimum RF output loads for device B1824-1C at 12 GHz.

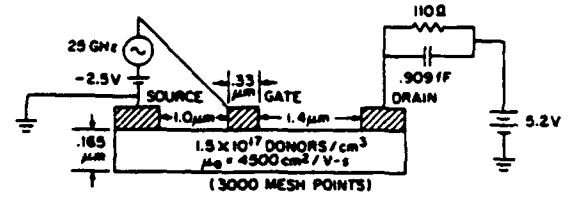


Fig. 18. Two-dimensional FET model parameters and the external circuits and voltage sources.

VII. Comparison of the Nonlinear Model with the Two-Dimensional FET Model

A direct comparison was made between the large-signal operation of the nonlinear FET model and that of an accurate two-dimensional (2-D) time-domain model for the GaAs FET. The 2-D model [17] includes carrier heating effects that produce velocity overshoot. In addition, the 2-D model produces voltage waveforms that are not restricted in harmonic content. Thus, it is possible to evaluate the accuracy of the nonlinear program with regard to the harmonic content of the voltage waveforms.

Fig. 18 shows the 2-D FET model and the external circuits and voltage sources. The gate is driven by a sinusoidal voltage source so negligible harmonic impedance will be assumed in the gate circuit for the nonlinear model. The drain load is 110 Ω shunted by a small capacitance to produce a time constant of 0.1 ps which is necessary to stabilize the solutions for the 2-D model. The FET is of short gate length (0.33 μm), high donor value (1.5×10^{17}/cm^3), and 100-μm width. The average current under the bias voltage shown is 20.0 mA, which makes the average drain voltage approximately 3.0 V. The input RF frequency is 25 GHz.

Time-domain simulations were made using the 2-D model and circuit for RF input voltage amplitudes of 0.75, 1.5, and 2.5 V. Each required considerable computational time.

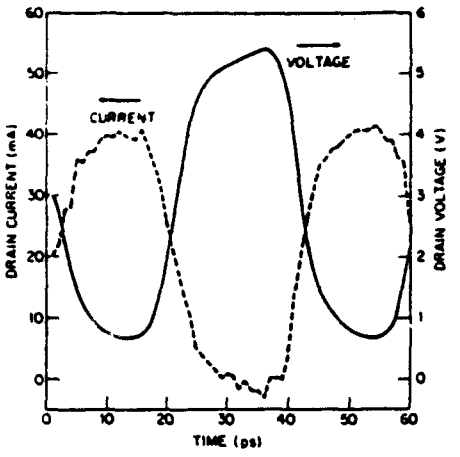


Fig. 19. Drain voltage and current waveforms for the two-dimensional FET simulation for gate-source ac amplitude of 2.5 V (Input power = 3.3 dBm).

Fig 19 shows the drain voltage and current waveforms for an input amplitude of 2.5 V. The simulation was made for one and one-half RF cycles. The voltage waveform can be seen to be repeating indicating that it is a steady-state waveform. The current is not calculated as accurately and has computational fluctuations that are not physically meaningful. The voltage waveform was then Fourier analyzed to find its harmonic content for comparison with the nonlinear model.

The nonlinear FET model was developed in the following manner. A small-signal equivalent circuit model was evaluated for the 2-D FET operated at a drain-source bias of 3.0 V. The elements values are:

$$R_{in} = 6.04$$
$$C_{gs} = 0.0461 \text{ pF}$$
$$C_{dg} = 4.90 \text{ fF}$$
$$g_m = 17.50 \text{ mS}$$
$$\tau = 0.5 \text{ ps}$$
$$R_{ds} = 5280\ \Omega$$
$$C_{ds} = 0$$
$$R_s = 5.1$$
$$R_g = 0$$
$$R_d = 0$$
$$L_{SOURCE} = 0.$$

The 2-D model was also used to calculate the steady-state drain current as a function of gate-source and drain-source voltages. The coefficients for analytic approximation of $I_{ds}(V_{in}, V_{out})$ were then evaluated. Avalanche breakdown and gate forward biasing were neglected.

Using these device parameters, the nonlinear FET amplifier program was operated assuming the RF load shown in Fig. 18. The solid lines in Fig. 20 are values of harmonic power delivered to the load as calculated by the

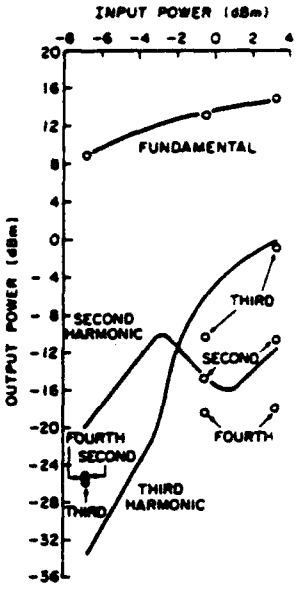


Fig. 20. Output power at fundamental-, second-, and third-harmonic frequencies as a function of input power. Solid lines are from NFET and points are from the two-dimensional model.

nonlinear program and the points are results of the 2-D simulations program.

The agreement is excellent for the fundamental output power. The agreement for second- and third-harmonic output power is good except at the lowest input power. Here the harmonic power calculation is clearly inaccurate in the 2-D program because all harmonic powers are the same, which is nonphysical. Only three harmonics are used in the nonlinear program so the fourth harmonic is not evaluated.

Notice particularly that the third-harmonic output power dominates in the FET. This effect has been observed experimentally by Willing *et al.* [11] and leads, we believe, to important third-order intermodulation distortion (IMD) in GaAs FET amplifiers. In fact, the IMD could be evaluated using the analytical model with some further programming effort.

Fig. 20 clearly shows that the nonlinear program accurately predicts saturation effects due to the nonlinear current control characteristic and also predicts harmonic power output accurately when harmonic impedances are accurately known. Once the parameters of the nonlinear model were known, it took 1/300 the computation time to generate the curves of Fig. 16 than it did to get the three cases with the 2-D model. The nonlinear model is clearly more efficient.

VIII. Conclusion

We have developed the FET model suitable for efficient calculation in the large-signal region. It is useful for developing optimized output network designs for high-power GaAs FET amplifiers. The program efficiency results from the use of the harmonic balance technique wherein the

nonlinear FET is analyzed in the time domain and the linear circuit is analyzed in the frequency domain.

The principle nonlinearities of the FET are voltage-controlled current sources. The nonlinearity of the reactive elements does not affect the large-signal solution greatly. However, it is necessary to evaluate the characteristics of the current sources for each device to be simulated. The simulation can be performed with a voltage waveform containing fundamental- and second-harmonic frequencies or fundamental-, second-, and third-harmonic frequencies. All FET current harmonics are included. The third harmonic is used only when accurate circuit impedance data is available at the third-harmonic frequency.

The nonlinear FET model was coupled to a program to generate constant output power contours on a Smith Chart. Excellent agreement was obtained with the measured load-pull characteristics at 12 GHz. However, the simulation predicted more gain than was measured in the experiments.

Finally, a comparison was made with large-signal simulations using an accurate 2-D model for the GaAs FET. This model includes carrier heating effects that produce the phenomenon of velocity overshoot. The output current and voltage waveforms in time could be directly compared for this case and the harmonic power contents were found to be in good agreement.

Appendix A
Dependence of the FET Parameters Upon Biasing

S-parameters were measured over a wide range of drain-source and gate-source voltages. The objective was to better understand the properties of the FET that contribute to good dc-to-RF power conversion. These measurements are useful because during large-signal operation, the device operating voltages have large excursion. Lumped-element circuit models were then constructed at each operating point.

The device tested (B1499-97) is capable of over 21-percent power-added efficiency at 20 GHz. Devices from this wafer have also operated at 35 GHz. This FET is representative of good but not the best of our devices.

Tables I and II show the values of the important equivalent circuit parameters as a function of gate-source voltage (Table I) and drain-source voltage (Table II). Although not presented here, we also have evaluated the circuit parameters at various gate-source voltages at $V_{ds} = 1$, 2 and 4 V. The parameters in the table are

- g_m transconductance,
- τ current delay time,
- C_{gs} gate-source capacitance,
- R_i gate-source resistance,
- C_{dg} drain-gate capacitance,
- R_{ds} drain-source resistance.

The following conclusions can be drawn from these measurements.

1) R_{ds} is a strong function of V_{ds} and V_{gs} and is approximately proportional to V_{ds}.

2) g_m is a strong function of both V_{ds} and V_{gs}.

TABLE I
FET Equivalent Circuit Parameters as a Function of Gate-Source Bias for Device B1499-#97. $V_{ds} = 8$ V

V_{gs} (V)	g_m (mS)	τ (ps)	C_{gs} (pF)	R_i (Ω)	C_{dg} (pF)	R_{ds} (Ω)
0	56.38	8.65	0.949	1.14	0.0141	515.2
-1	49.9	8.37	0.799	1.64	0.0200	422.9
-2	47.0	8.19	0.739	2.27	0.0259	326.2
-3	45.33	7.20	0.688	2.13	0.0327	269.1

TABLE II
FET Equivalent Circuit Parameters as a Function of Drain-Source Bias for Device B1499-#97. $V_{gs} = -2$ V

V_{ds} (V)	g_m (mS)	τ (ps)	C_{gs} (pF)	R_i (Ω)	C_{dg} (pF)	R_{ds} (Ω)
1	66.03	2.56	0.495	2.04	0.1993	22.4
2	63.97	3.11	0.607	1.82	0.0883	95.9
3	57.31	4.93	0.6614	1.65	0.050	171.3
8	47.00	8.19	0.739	2.27	0.0259	326.2

3) τ is a strong function of V_{ds} being approximately proportional to V_{ds}.

4) C_{dg} is a strong function of both V_{ds} and V_{gs}.

5) C_{gs} is a function of both V_{ds} and V_{gs}.

It is usually assumed that GaAs FET's follow a gate control characteristic resulting from a depletion depth calculable using a simple abrupt junction model. Neglecting source resistance, the saturated drain-source current I_{DS} is equal to

$$I_{DS} = I_p(1 - d/a)$$

where

- a active layer thickness,
- N_d donor value,
- Z gate width,
- v_s saturated election drift velocity,
- d depletion depth,
- V_{gs} gate-source voltage,
- V_{BI} built-in voltage,
- V_p pinchoff voltage ($qN_da^2/2\epsilon$),

and

$$d/a = \left[(V_{BI} - V_{gs})/V_p\right]^{1/2}$$

$$I_p = qN_dZav_s.$$

By differentiation of I_{DS}, the intrinsic transconductance g_m is

$$g_m = \epsilon Zv_s/d.$$

The gate-source capacitance C_{gs} is approximately equal to

$$C_{gs} = \epsilon ZL_g/d$$

where L_g equals gate length. (Parasitic capacitances external to the conduction channel are not included in C_{gs}.) If

TABLE III
FET AVERAGE VELOCITY CALCULATION AS A FUNCTION OF DRAIN-SOURCE BIAS VOLTAGE FOR DEVICE B1499-#97, $V_{gs} = -2$ V

V_{ds} (V)	$\tau_{tt} = C_{gs}/g_m$ (ps)	$v_s = L_g/\tau_{tt}$ (10^7 cm/s)
1	7.50	1.33
2	9.48	1.05
4	11.54	0.867
8	15.72	0.636

TABLE IV
FET AVERAGE VELOCITY CALCULATIONS AS A FUNCTION OF GATE-SOURCE VOLTAGE FOR DEVICE B1499-#97, $V_{ds} = 8$ V

V_{gs} (V)	I_{ds} (mA)	$\tau_{tt} = C_{gs}/g_m$ (ps)	$v_s = L_g/\tau_{tt}$ (10^7 cm/s)
0	190	16.83	0.594
-1	125	16.01	0.625
-2	95	15.72	0.636
-3	75	15.18	0.659

the transit-time under gate τ_{tt} is defined as L_g/v_s, then

$$\tau_{tt} = L_g/v_s = C_{gs}/g_m.$$

Notice that there is no obvious dependence upon drain-source voltage although real devices show the following several dependencies.

1) C_{gs} increases strongly as V_{ds} increases. This indicates a reduction in the depletion layer depth d, probably due to increased lateral diffusion due to increased electron energy.

2) The transconductance g_m decreases as V_{ds} increases. Since d is decreasing, the saturated velocity v_s must be decreasing significantly as V_{ds} is increased.

3) C_{gs}/g_m increases strongly as V_{ds} increases. This is due to the decreasing v_s with V_{ds} increase.

4) The time-delay factor for transconductance τ changes little with V_{gs} but increases directly as V_{ds}. Since τ must be directly related to τ_{tt}, this effect is also a result of v_s dependency upon V_{ds}.

We will now quantitatively interpret the FET measurements. Table III lists the calculated values of τ_{tt} and v_s as a function of V_{ds}. Table III shows that there is a strong dependence upon V_{ds}. However, the biasing power varies greatly during variation of V_{ds} so it is important to verify that average heating effects are not responsible for the changes in v_s.

Table IV shows v_s as a function of V_{gs}. Here also there is a large change in bias power. However, there is negligible change in v_s in Table IV. Therefore average temperature effects are not important in the results of Table I. The strong dependence of average electron drift velocity on drain-source voltage clearly influences the FET frequency response.

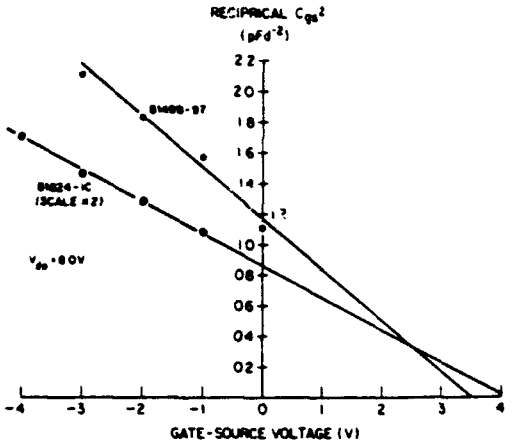


Fig. 21. Reciprocal gate-source capacitance squared as a function of gate-source voltage as determined from small-signal models for two laboratory devices.

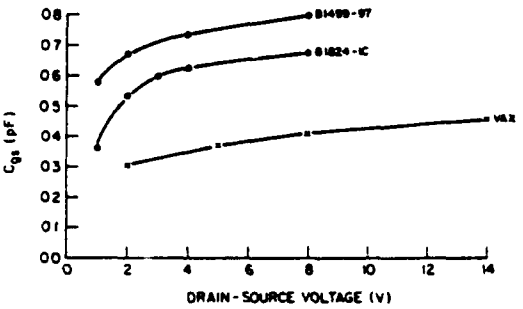


Fig. 22. Gate-source capacitance as a function of drain-source voltage as determined from small-signal measurements for two laboratory devices with $V_{gs} = -1$ V and for a two-dimensional simulation model with $V_{gs} = -2.75$ V.

APPENDIX B
GATE-SOURCE CAPACITANCE NONLINEARITY

The gate-source capacitance of a GaAs Schottky-barrier FET varies with both gate and drain voltage. However, measurements show that the variation is not large and it can often be neglected in nonlinear modeling.

Fig. 21 shows measured values of C_{gs}^{-2} plotted as a function of V_{gs}. The graphs are approximately linear as expected but the slopes are much less than expected. From the equations of Appendix A, it can be shown that, approximately

$$\frac{1}{C_{gs}^2} = \frac{2(V_{BI} - V_{gs})}{qNZ^2L_g^2}.$$

Separate measurements of the built-in voltage V_{BI} show it to be about 0.75 V. Since the above expression for C_{gs}^{-2} must go to zero value at $V_{gs} = V_{BI}$, we must conclude that there is significant fixed parasitic gate-source capacitance that is independent of the junction capacitance. This fixed capacitance reduces the percentage change in capacitance due to changes in V_{gs}.

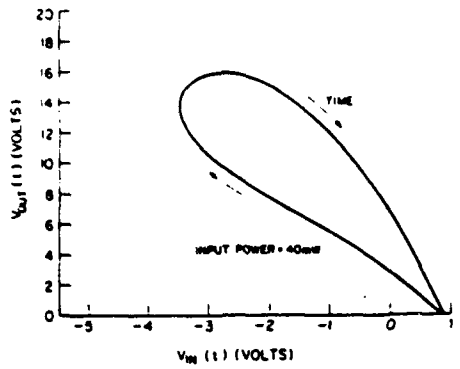


Fig. 23. Operating loci of input and output voltages for nonlinear simulations of FET B1512-3A with $V_{ds} = 8$ V, $V_{gs} = -1$ V, and output RF power = 154 mW.

Fig. 22 shows the variation in C_{gs} as a function of V_{ds} for two devices at $V_{gs} = -1$ V and for a 2-D model on the VAX 11/780 computer. All devices show an increase of C_{gs} with V_{ds}.

Clearly, C_{gs} increases with increase of V_{ds} and decrease of V_{gs}. However, in steady-state amplifier operation, V_{ds} is large when V_{gs} is small and vise-versa. Fig. 23 shows a typical relationship between V_{out} (or V_{ds}) and V_{in} (or V_{gs}) for large-signal operation of a typical device, as calculated by the nonlinear program. Based upon the measured data we assumed that

$$C_{gs} = 0.909\left[1 + 0.0125\, V_{out}(t)\right]\sqrt{\frac{3.75 - V_{gs}^{dc}}{3.75 - V_{in}(t)}} \cdot C_0$$

where C_0 is the value of C_{gs} at V_{gs}^{dc} and $V_{ds} = 8.0$ V. The variation for C_{gs} over the operating path of Fig. 23 as given by the above equation is less than 20 percent. This is the reason that nonlinear simulations that assume a fixed value of capacitance give very nearly the same solutions for RF power computations.

Acknowledgment

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GaAs FET Device and Circuit Simulation in SPICE

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Abstract—We have developed a GaAs FET model suitable for SPICE circuit simulations. The dc equations are accurate to about 1 percent of the maximum drain current. A simple but accurate interpolation formula for drain current as a function of gate-to-source voltage connects the square-law behavior just above pinchoff and the square-root law for larger values of the drain current.

The ac equations, with charge-storage elements, describe the variation of the gate-to-source and gate-to-drain capacitances as the drain-to-source voltage approaches zero and when this voltage becomes negative. Under normal operating conditions the gate-to-source capacitance is much larger than the gate-to-drain capacitance. At zero drain-to-source voltage both capacitances are about equal. For negative drain-to-source voltages the original source acts like a drain and vice versa. Consequently the normally large gate-to-source capacitance becomes small and acts like a gate-to-drain capacitance. In order to model these effects it is necessary to realize that, contrary to conventional SPICE usage, there are no separate gate-to-source and gate-to-drain charges, but that there is only one gate charge which is a function of gate-to-source and gate-to-drain voltages. The present treatment of these capacitances permits simulations in which the drain-to-source voltage reverses polarity, as occurs in pass-gate circuits.

I. Introduction

IN ANY INTEGRATED circuit design one usually starts with a computer simulation of the circuit to be built. If the circuit consists of not more than a few hundred devices then the well-known program SPICE, originally developed at the University of California, Berkeley, is often used. While SPICE can model transistors at different levels of complexity and usually gives answers with great reliability, it was written originally for silicon devices only. In principle, the physics of Si junction FET's is very similar to GaAs FET's. Some of the differences are that in GaAs one usually deals with a Schottky-barrier junction instead of a p–n junction, and also in GaAs the conducting channel is confined on one side by a space-charge region and on the other side by a semi-insulating region. In Si the channel is usually, but not always, constricted from both sides by space-charge regions formed around the gate p–n junctions. Thus one might expect that both types of devices could be modeled by the same equations. This unfortunately cannot be done. The physical reason for this dissimilarity lies in the fact that in GaAs the electron velocity saturates near the rather low electric field of 3×10^3 V/cm whereas Si obeys ohmic behavior over a range approximately ten times larger. Thus in GaAs the saturation of drain current with increasing drain-to-source voltage is caused by carrier-velocity saturation, whereas in silicon it is channel pinchoff that causes the drain current to saturate.

The equations derived at this laboratory in [1] and [2] are rather accurate and generally more accurate than those used in the SPICE program. However, the resulting expressions are very complex and would execute too slowly in a practically useful SPICE implementation. The challenge then presented to us consisted of finding simple expressions that execute quickly but at the same time are accurate enough to give reliable circuit simulations.

II. The DC Equations

Recently a publication appeared [3] in which the dc equations exclusive of parasitic resistances are approximated by

$$I_d = \beta(V_{gs} - V_T)^2 (1 + \lambda V_{ds}) \tanh (\alpha V_{ds}). \quad (1)$$

In this equation, I_d is the drain current, β is a parameter, V_{gs} is the gate-to-source voltage, V_{ds} is the drain-to-source voltage, V_T is the threshold voltage, λ is a parameter related to drain conductance, and α determines the voltage at which the drain current characteristics saturate. Note that the drain current saturates at the same drain-to-source voltage irrespective of the gate-to-source voltage. This is different from conventional JFET or MOSFET models and occurs because the critical field E_{sat} in the channel is reached at approximately the same voltage $V_{ds} = E_{sat} \times L$, where L is the channel length. When comparing [1] against experiment, we found that the expression is a good representation of the current for a given V_{gs}. However, the behavior of I_d as a function of V_{gs} is only poorly represented, especially if the pinchoff voltage of the transistor is large. Our earlier work had shown that, except for V_{gs} near the pinchoff voltage, the saturated drain current I_{ds} is proportional to the height of the undepleted channel region near the source end. This is because the reduction in channel height between the channel entrance and the point where the carrier velocity saturates is usually a negligible fraction of the height at the entrance. Thus the current may be approximately calculated by assuming that all carriers at the channel opening are moving at their saturated velocity. For constant channel doping, the saturated drain current I_{ds} should then vary approximately as

$$I_{ds} = Z v_{sat} \sqrt{2\epsilon q N_d} \left(\sqrt{(-V_T + V_B)} - \sqrt{(-V_{gs} + V_B)}\right) \quad (2)$$

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where Z is the channel width, v_{sat} is the saturated electron velocity, ϵ is the dielectric constant, q is the electron charge, N_d is the donor density, V_T is the threshold or pinchoff voltage, and V_B is the built-in potential of the gate junctions. Note that V_{gs} and V_T are normally negative. The first term in (2) is proportional to the height of the space-charge region at the threshold voltage, and thus is proportional to the thickness of the doped region under the gate. The second term in (2) is proportional to the height of the space-charge region when the gate-to-source voltage V_{gs} is applied. Thus (2) is indeed proportional to the height of the undepleted channel.

The full (2) is obtained by assuming that all carriers in the channel opening move at their saturated velocity. The approximation for the current in (2) breaks down when the voltage drop from the entrance of the channel to the point of velocity saturation of the carriers is comparable to the voltage difference $V_{gs}-V_T$. Under these conditions the assumption of constant channel height breaks down. We may get an idea of the magnitude of this critical voltage by considering an example. Let us assume that we are dealing with an FET with a 1-μm channel length. Obviously the length under the channel where the carriers move at their unsaturated velocity has to be less than the total gate length. The electric field strength along the same portion of the channel has to be less than E_{sat} because the carriers are moving at less than saturated velocity. Thus an upper limit of the voltage drop along the channel, before the carriers become saturated, is $E_{sat}L$, where L is the total channel length. For the known value of E_{sat} of about 3×10^3 V/cm, the above critical voltage drop becomes 0.3 V or less. Hence, we thus expect that the above approximation in (2) is not valid when $|V_{gs} - V_T| \leq 0.3$ V. In the limit of gate voltages near the pinchoff point, the equations of [1] and [2] lead to a quadratic law

$$I_{ds} \sim \beta(V_{gs} - V_T)^2. \tag{3}$$

This situation is similar to what is found in the conventional JFET model. The derivation of (3) from the expressions in [1] and [2] is not shown here. Unfortunately, (3) is valid only near $V_{gs} - V_T = 0$. Elsewhere the behavior is better described by (2). To illustrate the theoretical expectations of [1] and [2], we have programmed the relevant equations on a computer and show in Fig. 1(a) and (b) I_{ds} versus V_{gs} for transistors with pinchoff voltages of -0.5 and -2.5 V, respectively. As may be seen, the curves start quadratically but soon change and follow more of a square-root-like behavior as exhibited by (2).

To smoothly connect a law like (3) for small $V_{gs} - V_T$ to an expression like (2) for larger $V_{gs} - V_T$, we chose the empirical expression

$$I_{ds} = \frac{\beta(V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)}. \tag{4}$$

For small values of $V_{gs} - V_T$, the expression is indeed quadratic while for larger values, I_{ds} becomes almost linear in $V_{gs} - V_T$. The denominator in (4) is new and it has not been used, to our knowledge, by the modeling community. Note that the expressions derived in [1] and [2] apply to a truly abrupt interface between the active layer and the undoped buffer. In Fig. 1(a) and (b) we show by a solid line a fit based on (4). The b values found are 2.6 and 1.5 V^{-1}, respectively. The situation becomes more complicated when one considers that in all practical devices there is a gradual transition in doping from the channel into the buffer caused by diffusion and/or implant-produced doping tails. Because of this diffuse channel edge, the depletion region quickly expands as the pinchoff point is approached. The transconductance at any one point is approximately inversely proportional to the distance between the gate and the channel edge. Real doping profiles then produce curves of I_{ds} versus V_{gs} which rise more gradually than calculated in [1] and [2]. Interestingly, we find that the empirical expression (4) still describes actual transistor characteristics exceptionally well, but with changed parameters β and b. The more gradual doping profiles appear to give a lower value of b. To illustrate this point, we show in Fig. 1(c) and (d) measured characteristics for both implanted devices and transistors made on epitaxial material. We find that (4) is accurate and the error is usually less than 1-percent of the maximum current. In Fig. 1(c) we depict a device made in MBE material, and (4) is seen to be a good approximation over most of the range. Fitting the expression (4) to experiment requires a value of $b = 0.45$ V^{-1}. Furthermore Fig. 1(c) shows $(I_d)^{1/2}$ rather than I_d to better illustrate the behavior at low drain currents. We also show the above discussed approximations based on (2) with the square-root law, and (3) using the square law. It is evident that the new model fits the data much better than either of the other two approximations alone. Transistors produced by our standard digital process are shown in Fig. 1(d). They use an implanted channel in conjunction with a recessing gate etch, and thus have a more gradual profile. Their b-value is about 0.3 (see Fig. 1(d)). The values quoted for b refer to a bare transistor without parasitic source and drain resistors. In extracting the characteristics of a bare transistor from measured ones, there is always some uncertainty about the values of the parasitic resistors, and the values of b reflect these uncertainties. Interestingly, (4) is rather forgiving, permitting good fits to transistor curves even when the parasitic resistors are not extracted. The values of β and b are, however, different in these cases.

The value of b of the bare transistor is a measure of the doping profile extending into the insulating substrate and thus depends on the fabrication process. Neglecting b cannot be tolerated in most circuit simulations.

We also found that the tanh function in (1) consumes considerable computer time. We further approximated the tanh function below saturation by a simple polynomial P of the form

$$P = 1 - \left(1 - \frac{\alpha V_{ds}}{n}\right)^n, \quad \text{with } n = 2 \text{ or } 3. \tag{5}$$

In the saturated region ($V_{ds} > n/\alpha$), the tanh function is

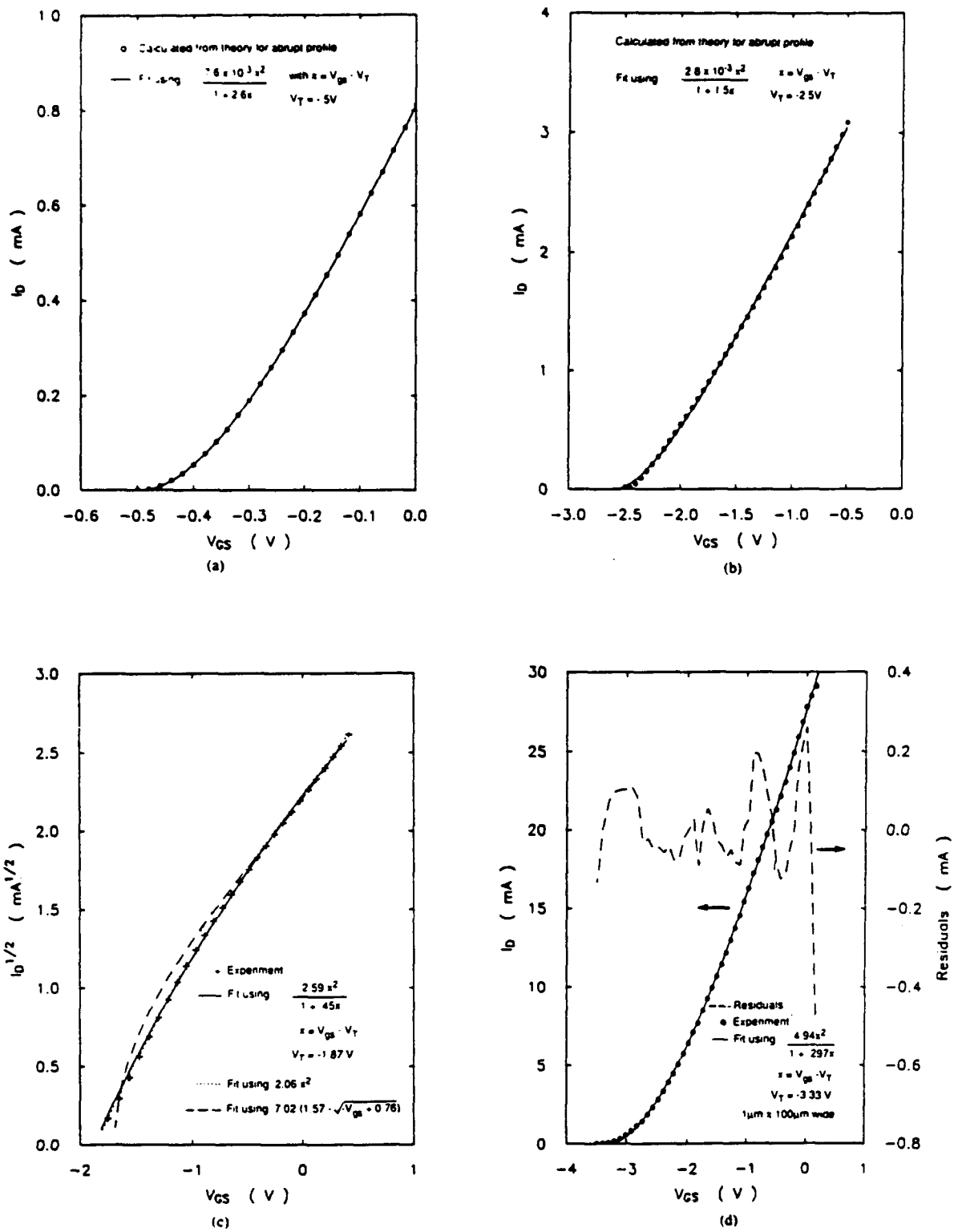

Fig. 1. Saturated drain current I_{ds} versus gate-to-source voltage V_{gs}, and comparison with simplified model predictions for various cases: (a) Theoretical characteristics for an abrupt profile with a pinchoff voltage of −0.5 V and a 1 × 20 μm gate. There are no parasitic source and drain resistors. (b) Same but with pinchoff voltage of −2.5 V. (c) Experimentally measured characteristics for a transistor with a 1 × 20 μm gate and a rather abrupt doping profile fabricated on MBE-grown epitaxial material. The plot also shows in addition the comparison with two other approximate models as explained in the text. We plot here $(I_d)^{1/2}$ instead of I_d to show more clearly the model comparisons in the low current region. The experimental curves represent a "bare" transistor without parasitic source and drain resistors. (d) Measured characteristics for an FET made by ion-implantation followed by a gate recessing etch. Gate dimensions are 1 × 100 μm. The curves have been corrected for source and drain resistors.

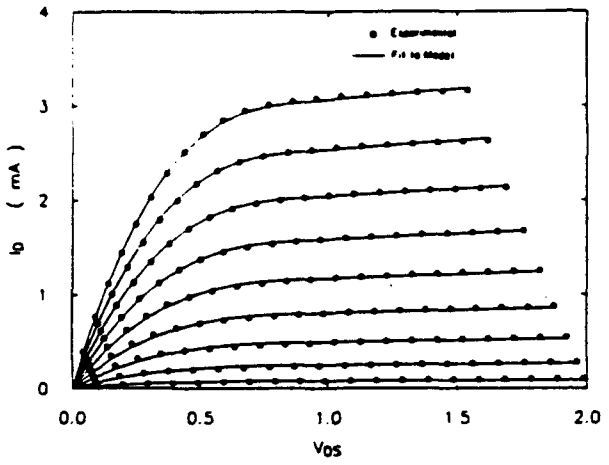

Fig. 2. Drain current I_d versus drain voltage V_{ds} for an experimental FET, and the approximation representing the polynomial model with $n = 3$.

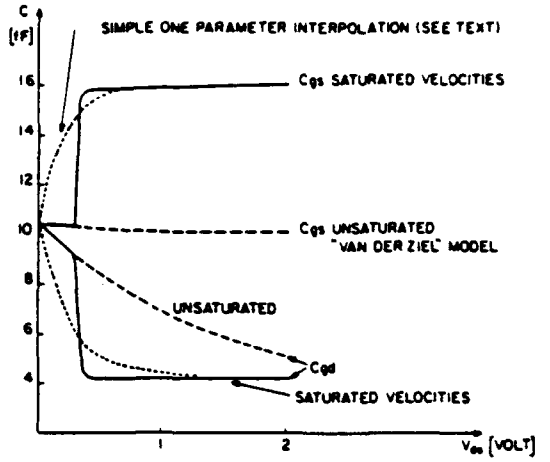

Fig. 3. Gate-to-source and gate-to-drain capacitances for a 1 × 20 μm gate on GaAs with 1×10^{17} donors/cm^3. The figure shows the unsaturated model of van der Ziel (long dashes), the saturated velocity model (solid lines), and a simple one-parameter interpolation (short dashes) as discussed in the text.

replaced by unity. This is similar to what is done in the conventional SPICE program.

The slope at $V_{ds} = 0$ of the polynomial is α and is equal to that of the $\tanh(\alpha V_{ds})$ function. While the tanh function and the two-section approximations with $n = 2$ or 3 all give good fits to experimentally measured curves, we found consistently that the polynomial with $n = 3$ gives the best fit. Note that for $n = 3$ the two-section function has first and second derivatives which are continuous for all $V_{ds} > 0$. In making comparisons with experiments, as in Fig. 2, the experimental curves are corrected for voltage drops across the parasitic resistors between source and gate as well as gate and drain. No allowance has been made for the fact that these resistors change as the gate-to-source voltage is varied, owing to the constriction of the current flow to and from the variable height channel.

In summary, we have modified the code in SPICE to include a GaAs model with the following dc equations:

$$I_d = \frac{\beta(V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)} \left\{1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3\right\} (1 + \lambda V_{ds}),$$

$$\text{for } 0 < V_{ds} < \frac{3}{\alpha} \tag{6a}$$

$$I_d = \frac{\beta(V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)} (1 + \lambda V_{ds}),$$

$$\text{for } V_{ds} \geq \frac{3}{\alpha}. \tag{6b}$$

III. Source and Drain Capacitance

Source and drain capacitance models have been considered in the literature [2], [6]–[9]. Current GaAs device simulations use a diode-like capacitance between source and gate, where the space-charge region thickness and thus the capacitance is determined by the gate-to-source voltage. A similar diode model is often used to describe the normally much smaller gate-to-drain capacitance. These approximations have serious shortcomings. Consider, for example, the case of zero source-to-drain voltage. From the symmetry of the physics of the FET one concludes that the gate-to-source and gate-to-drain capacitances should be equal, yet the above model says that they may be very different. Even worse inaccuracies are encountered when the transistor is reverse-biased, i.e., when the drain really acts like a source, and the source acts like a drain. Now the model says that the large capacitance is still between the original source and gate while in reality the big capacitance is now between the original drain and gate. Thus, large errors can be introduced into simulations when low source-to-drain voltages or reverse-biased transistors are encountered, as in transmission gate circuits.

While the above objections apply to both Si and GaAs devices, the behavior for GaAs is further complicated by the early onset of carrier-velocity saturation. Let us briefly review some of the underlying theory. Van der Ziel [6] calculated capacitances for FET's without including effects of velocity saturation. In Fig. 3 we show the unsaturated velocity values of C_{gs} and C_{gd} as a function of V_{ds} for $V_{gs} = 0$ V. The channel is assumed to have a doping of 1×10^{17} donors/cm^3 and the gate has dimensions of 1 × 20 μm with $V_B = 0.8$ V. It is seen that C_{gs} is approximately constant as a function of V_{ds}. While we have not shown the capacitance curves for V_{gs} not equal to zero, they follow approximately the diode capacitance model as a function of V_{gs}. This is presumably the basis for the diode-like behavior programmed into Si JFET devices. The gate-drain capacitance C_{gd} starts at the same value as C_{gs} for $V_{ds} = 0$. It then falls continuously with increasing V_{ds} and goes to zero when the drain side of the channel becomes pinched off.

When velocity saturation is taken into account, the situation changes drastically. In [2], the total junction capacitance between the gate and the rest of the device is

derived. These results can be readily extended to calculate C_{gs} and C_{gd} separately by taking the partial derivatives of the total gate charge with respect to gate-source and gate-drain potentials. For the convenience of the reader, we summarize these capacitance expressions in the Appendix, including those previously unpublished. Evaluating the resulting saturated velocity expressions gives a gate-to-source capacitance that rises rather abruptly from the van der Ziel model at the onset of saturation and quickly approaches a nearly constant value as a function of V_{ds}. Similarly the gate-to-drain capacitance drops abruptly to a low value and then stays approximately constant. In reality one may expect that the transition to the saturated velocity capacitance model is not quite as abrupt because the onset of velocity saturation of the carrier is also more gradual. There are almost no published data on C_{gs} and C_{gd} for GaAs FET's. However, the few data available indicate qualitative agreement with these models.

An additional problem is encountered in the SPICE code. The integration routines require from the device model separate closed-form expressions for the source-to-gate charge and gate-to-drain charge. These charges are used in the program to calculate displacement currents due to finite voltage steps. For these displacement currents, the absolute values of the charges are immaterial but their changes are of importance. Since in the real device there are no separate gate-drain or gate-source charges but only one gate charge, which is a function of V_{gs} and V_{gd}, we choose to set the initial values of each of these charges in the code, during a simulation, to half of the total gate charge Q_g. Each charge is then incremented when the voltage levels change. In the case of the gate-to-source charge Q_{gs} we take

$$\Delta Q_{gs} = Q_g(V_{gs} + \Delta V_{gs}, V_{gd}) - Q_g(V_{gs}, V_{gd}). \quad (7a)$$

This formula may be generalized if simultaneously both voltages V_{gs} and V_{gd} change by ΔV_{gs} and ΔV_{gd} by averaging (7a) over the two values of V_{gd}.

$$\Delta Q_{gs} = \tfrac{1}{2}(Q_g(V_{gs} + \Delta V_{gs}, V_{gd} + \Delta V_{gd}) - Q_g(V_{gs}, V_{gd} + \Delta V_{gd}) + Q_g(V_{gs} + \Delta V_{gs}, V_{gd}) - Q_g(V_{gs}, V_{gd})). \quad (7b)$$

This definition for the gate-source charge is somewhat artificial, but the displacement currents calculated from the above expressions should be rather accurate. An analogous equation can be written down for ΔQ_{gd}

$$\Delta Q_{gd} = \tfrac{1}{2}(Q_g(V_{gs} + \Delta V_{gs}, V_{gd} + \Delta V_{gd}) - Q_g(V_{gs} + \Delta V_{gs}, V_{gd}) + Q_g(V_{gs}, V_{gd} + \Delta V_{gd}) - Q_g(V_{gs}, V_{gd})). \quad (7c)$$

Equations (7b) and (7c) are still approximations, albeit very good ones. However, note that the total gate-charge changes are calculated exactly. This may be seen by calculating, with the help of (7b) and (7c), the total change ΔQ_g in the gate charge due to a simultaneous voltage change in both V_{gs} and V_{gd}

$$\Delta Q_g = \Delta Q_{gs} + \Delta Q_{gd} = Q_g(V_{gs} + \Delta V_{gs}, V_{gd} + \Delta V_{gd}) - Q_g(V_{gs}, V_{gd}) \quad (8)$$

which is obviously an exact result.

A major challenge is to find a simple expression for the gate charge Q_g. Measurements as well as calculations based on [2] confirm that the gate-source capacitance C_{gs} is approximated by a simple diode-capacitance model, in the normal bias range $V_{ds} >> 0$. The gate-to-drain capacitance C_{gd} in this voltage range is small as compared to C_{gs} ($C_{gd} = 0.1 - 0.3\ C_{gs}$), and furthermore, C_{gd} is approximately constant and nearly independent of V_{gs} or V_{gd}.

We may thus choose a gate charge (for constant doping under the gate) and for a normally (forward) biased transistor

$$Q_g = 2\ C_{gs0} V_B \left(1 - \sqrt{1 - \frac{V_{gs}}{V_B}}\right) + C_{gd0} V_{gd} \quad (9a)$$

for $V_{ds} >> 0$, or alternatively, $-V_{gd} >> -V_{gs}$. (The use of $-V_{gs}$ and $-V_{gd}$ instead of V_{gs} and V_{gd} allows for the fact that both voltages are usually negative, and it is usually easier to think in terms of positive quantities.)

In (9a), C_{gs0} is the gate-to-source capacitance for zero source-to-gate bias, V_B is the built-in junction potential and C_{gd0} is the gate-to-drain capacitance. The charge has been normalized to be zero when $V_{gs} = 0$ and $V_{gd} = 0$. Note that V_{gs} is negative in the normal bias range. The first part of (9a) follows directly from Poisson's equation and is identical to the form used in SPICE.

For a reverse-biased transistor ($V_{ds} << 0$), different equations are needed, since the nominal source now really acts like a drain and the nominal drain like a source. The corresponding charge expression, obtained by interchanging V_{gd} and V_{gs}, is

$$Q_g = 2C_{gs0} V_B \left(1 - \sqrt{1 - \frac{V_{gd}}{V_B}}\right) + C_{gd0} V_{gs} \quad (9b)$$

for $V_{ds} << 0$ or alternatively $-V_{gd} << -V_{gs}$.

The transition from (9a) to (9b) can be envisioned to occur at $V_{ds} = 0$, or $V_{gd} = V_{gs}$. At $V_{ds} = 0$, Q_g is continuous, as may be seen by inspection. The derivatives of Q_g with respect to the voltages, however, are discontinuous. In particular, we find for $V_{ds} > 0$

$$C_{gs} = \frac{dQ_g}{dV_{gs}} = \frac{C_{gs0}}{\sqrt{1 - \frac{V_{gs}}{V_B}}}$$

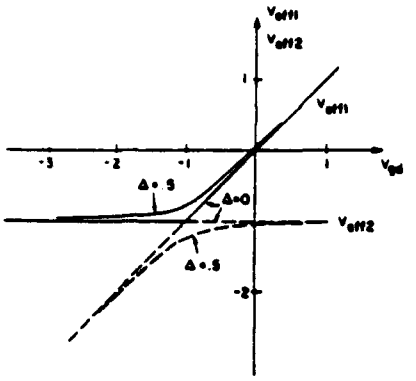

Fig. 4. V_{eff1} and V_{eff2} for $V_{gs} = -1$ V as a function of V_{gd} from -4 to $+2$ V for $\Delta = 0$ and 0.5.

$$C_{gd} = \frac{dQ_g}{dV_{gd}} = C_{gd0} \tag{10}$$

and for $V_{ds} < 0$

$$C_{gs} = \frac{dQ_g}{dV_{gs}} = C_{gs0}$$

$$C_{gd} = \frac{dQ_g}{dV_{gd}} = \frac{C_{gs0}}{\sqrt{1 - \dfrac{V_{gd}}{V_B}}}.$$

Equation (10) approximates the desired behavior but is still deficient in that the abrupt transitions or steps in the values of C_{gs} and C_{gd} at $V_{ds} = 0$ are nonphysical and also would cause convergence difficulties in the numerical analysis.

Let us next address the achievement of a gradual transition of the capacitance values near $V_{ds} = 0$. Note that (9a) and (9b) can be written in the form

$$Q = 2C_{gs0}V_B\left(1 + \sqrt{1 - \frac{V_{eff1}}{V_B}}\right) + C_{gd0}V_{eff2}. \tag{11}$$

Here $(-V_{eff1})$ is meant to stand for the smaller of the two values of $(-V_{gd})$ or $(-V_{gs})$ and $(-V_{eff2})$ for the larger of the two. Mathematically, we can select these values by using the functions

$$V_{eff1} = \tfrac{1}{2}\{V_{gs} + V_{gd} + \sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}\} \tag{12a}$$

$$V_{eff2} = \tfrac{1}{2}\{V_{gs} + V_{gd} - \sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}\} \tag{12b}$$

with $\Delta = 0$. The inclusion of a nonzero Δ produces a smooth transition of width Δ in the value of V_{eff1} and V_{eff2} as a function of V_{gs} or V_{gd}. To illustrate (12), we plot in Fig. 4 V_{eff1} and V_{eff2} for $V_{gs} = -1$ V as a function of V_{gd} from -4 to 2 V for $\Delta = 0$ and 0.5.

The use of V_{eff1} and V_{eff2} in (12) also yields a smooth interpolation of C_{gs} and C_{gd} through the former point of discontinuity at $V_{ds} = 0$. Differentiating (11) gives

$$C_{gs} = \frac{C_{gs0}}{\sqrt{1 - \dfrac{V_{eff1}}{V_B}}}\frac{1}{2}\left\{1 + \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}}\right\} + C_{gd0}\frac{1}{2}\left\{1 - \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}}\right\} \tag{13a}$$

$$C_{gd} = \frac{C_{gs0}}{\sqrt{1 - \dfrac{V_{eff1}}{V_B}}}\frac{1}{2}\left\{1 - \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}}\right\} + C_{gd0}\frac{1}{2}\left\{1 + \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}}\right\}. \tag{13b}$$

As already stated, the charge Q_g should not change if the values of V_{gs} and V_{gd} are interchanged, to reflect the symmetry of the transistor. Equations (11) and (12) satisfy this condition.

The transition width Δ has the dimensions of a voltage and is an adjustable parameter. Its magnitude is related to the voltage at which velocity saturation is reached. Studies based on Fig. 3 and the analysis of [1] and [2] show the establishment of a velocity-saturated zone under the gate for voltages V_{ds} just above the onset of velocity saturation. The length of the velocity-saturated zone depends only weakly on V_{ds}. Both the capacitances C_{gs} and C_{gd} as well as the drain current stabilize near the same voltage point (see Fig. 3). Further increases in drain voltage only weakly affect their values. From (2) and (6), $V_{ds} = 1/\alpha$ describes the onset of drain-current saturation. In accordance with the above reasoning we shall use in the following $\Delta = 1/\alpha$. This interpolation is shown by the dashed line in Fig. 3. Compare it to calculations based on the model of [2]. There is obviously room for more elaborate approximations to reproduce the fine structure of the capacitance at small voltages.

We have plotted, in Fig. 5, C_{gs} from (13a), for V_{ds} between 4 and -4 V and $V_{gs} = 0$, -1, -2, and -3 V, to illustrate the behavior of the gate-to-source capacitance in our model. For positive V_{ds} (normal operating mode) the gate-to-source capacitance shows the capacitance behavior of a diode with voltage V_{gs}. In the reverse-biased direction ($V_{ds} < 0$), the gate-to-source capacitance approaches C_{gd0}. The transition region width from high to low capacitance has a value of about $1/\alpha$, as chosen above.

The plot for negative V_{ds} is somewhat confusing. Along any one curve V_{gs} is a parameter and held constant. However, for negative V_{ds}, V_{gd} and not V_{gs} becomes the important gate voltage, because of the discussed role reversal of source and drain. V_{gs} is kept constant along one curve and V_{gd} varies with V_{ds}. Thus for negative drain-to-source voltages the "effective drain" may be thought of being tied through a battery to the gate. Furthermore, for large negative V_{ds}, V_{gd} (the "effective V_{gs}") becomes positive. Each of the plotted capacitance curves is carried to

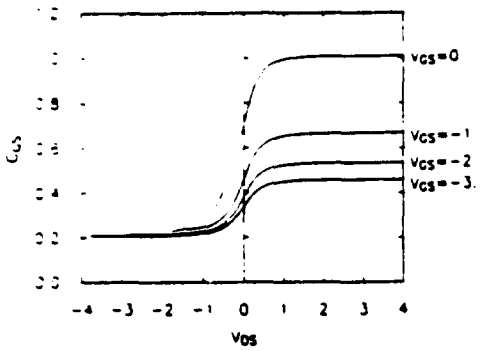

Fig. 5. Gate-to-source capacitance for V_{ds} between +4 and −4 V and V_{gs} = 0, −1, −2, and −3 V. Note for negative drain-to-source voltages, the capacitance approaches the small gate-to-drain capacitance.

the point where V_{gd} becomes +0.5 V. This brings us to another important point, namely the well-known singularity in the junction capacitance when the depletion region thickness collapses to zero.

Positive junction voltages with values of V_B or larger give rise, in the present approximation, to nonphysical infinite or complex capacitances. In order to avoid imaginary numbers or dividing by zero in (7)–(13), when V_{eff1} becomes positive and equal to or larger than V_B, we limit the values of V_{eff1} to a maximum value of V_{max}. In the following we have chosen V_{max} to be 0.5 V. This procedure limits the value of the junction capacitance; the particular choice of V_{max} determines its maximum value. For voltages beyond V_{max}, we take the capacitance to remain constant. This is similar to a more elaborate approach used by Poon and Gummel [8]. There exist no good models that would indicate what the capacitance should be for voltages beyond V_{max} and near V_B. As pointed out in [8], this detailed behavior is probably not important because the large forward currents of the junction, in this voltage region, are larger than the displacement currents. If this region were to be modeled more accurately, a distinction between Schottky-barrier and p–n junction gates would have to be made: The Schottky-barrier junction would not exhibit the large diffusion capacitance associated with minority-carrier injection.

As stated above, the gate-to-source capacitance would go to infinity for $V_{eff1} = V_B$. We now keep the capacitance constant, when $V_{eff1} > V_{max}$, by using the following function for Q_g:

$$Q_g = C_{gs0}\left\{2V_B\left(1-\sqrt{1-\frac{V_{max}}{V_B}}\right)+\frac{V_{eff1}-V_{max}}{\sqrt{1-\frac{V_{max}}{V_B}}}\right\} + C_{gd0}V_{eff2}, \text{ for } V_{eff1} \geqq V_{max}. \quad (14)$$

IV. Capacitance Beyond The Pinchoff Point

When FET is pinched off, the gate-to-source junction capacitance falls to a small value, usually determined by the sidewall capacitance of the space-charge region. Simply setting the capacitance C_{gs} equal to zero would cause a discontinuity and result in convergence problems in the simulations. We thus once more use the smooth interpolation that we employed in (12) and (13). Accordingly, we introduce a V_{new} that is to be essentially equal to V_{eff1} before pinchoff and to V_T beyond pinchoff. In other words, V_{new} is to select the smaller of the two values of $-V_T$ and $-V_{eff1}$. Applying the procedure of (12) once more gives

$$V_{new} = \tfrac{1}{2}(V_{eff1} + V_T + \sqrt{(V_{eff1} - V_T)^2 + \delta^2}) \quad (15)$$

where δ represents the voltage range over which the transition between these two values is accomplished, as above. In our simulations, we arbitrarily use $\delta = 0.2$ volts. Introducing the function of (15), in place of V_{eff1}, into (11), one may again calculate, through partial differentiation, the values of C_{gs} and C_{gd}.

$$C_{gs} = \frac{C_{gs0}}{\sqrt{1-\frac{V_{new}}{V_B}}}\frac{1}{2}\left\{1+\frac{V_{eff1}-V_T}{\sqrt{(V_{eff1}-V_T)^2+\delta^2}}\right\} \times \frac{1}{2}\left\{1+\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} + C_{gd0}\frac{1}{2}\left\{1-\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} \quad (16)$$

$$C_{gd} = \frac{C_{gs0}}{\sqrt{1-\frac{V_{new}}{V_B}}}\frac{1}{2}\left\{1+\frac{V_{eff1}-V_T}{\sqrt{(V_{eff1}-V_T)^2+\delta^2}}\right\} \times \frac{1}{2}\left\{1-\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} + C_{gd0}\frac{1}{2}\left\{1+\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} \quad (17)$$

Similarly V_{eff1} in (14) should also be replaced by V_{new}.

In Fig. 6 we illustrate the behavior of C_{gs} from (16) as a function of V_{gs} and for various source-to-drain voltages. For $V_{ds} >> 0$ (normal biasing conditions,) C_{gs} follows a diode-like capacitance model as a function of V_{gs}. However, when V_{gs} approaches the pinchoff voltage V_T, C_{gs} falls rapidly to zero within a voltage range δ. For V_{ds} negative, C_{gs} is really a gate-to-drain capacitance because the reverse bias interchanges the roles of source and drain. The capacitance in this range becomes small and independent of V_{gs}. Because of the smooth transition from posi-

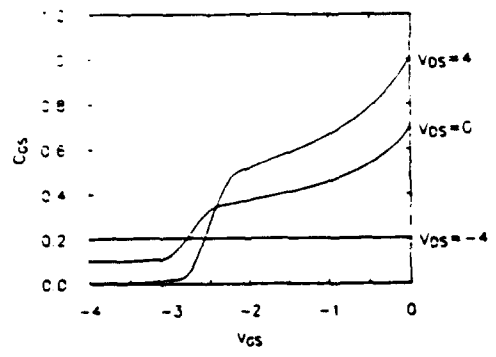

Fig. 6. This figure illustrates how, in the presented model, the gate-to-source capacitance behaves as V_{gs} goes through the pinchoff point V_T (here equal to -2.5 V).

tive to negative drain-to-source voltages, the situation for $V_{ds} = 0$ is intermediate between the two cases outlined above.

Code changes based on the above equations have been introduced into the SPICE code. Satisfactory circuit simulations without convergence problems have been obtained.

The above models may be further refined as more experience is obtained from their use and as deficiencies or inaccuracies become apparent.

Appendix

We shall summarize expressions for the gate–source and gate–drain capacitances C_{gs} and C_{gd}. For completeness we shall first repeat the expressions of van der Ziel [6] which are valid when the carrier velocity is unsaturated. The nomenclature is essentially that of [2]. With the voltage sign conventions corresponding to an n-type FET with a Schottky-barrier (or p-type) gate, we introduce the following reduced potentials and definitions:

$$W_{oo} = -V_T + V_B = \frac{qN}{2\epsilon} a^2 \tag{A1}$$

$$W_s = -V_{gs} + V_B \tag{A2}$$

$$s = \sqrt{\frac{W_s}{W_{oo}}} \tag{A3}$$

$$d = \sqrt{\frac{-V_{gs} + V_B + V_d}{W_{oo}}} \tag{A4}$$

$$p = \sqrt{\frac{-V_{gs} + V_B + V_p}{W_{oo}}}. \tag{A5}$$

In the above, W_{oo} is a positive quantity corresponding to the total voltage (including built-in voltage) needed to pinchoff the undepleted channel of thickness a, with doping density N. Furthermore, q is the electronic charge and ϵ is the dielectric constant of GaAs. W_s is again usually positive and represents the total voltage difference, including built-in voltage between the gate and the source end of the channel. The quantity s is defined in (A3). By replacing W_s in it by the total voltage between the gate and the drain end of the channel, the quantity d is obtained; by using instead of W_s the total voltage between the gate and the channel at the point of velocity saturation, the quantity p is obtained. The parameter p is only needed when the carrier velocities become saturated. It has to be calculated for each s value, utilizing [2]. Typically one uses the equation for V_{ds}, which is a function of s and p. It results in a transcendental equation for p as a function of s and V_{ds}. The gate-to-source voltage specifies s as seen in (A3), p is then determined for each given V_{ds}.

In the "van der Ziel" or unsaturated velocity regimes [6]

$$C_{gs} = \epsilon Z \frac{2L}{a} \frac{[\frac{2}{3}(d^3 - s^3) - \frac{1}{2}(d^4 - s^4)](1 - s) - f_1(s, d)(s - s^2)}{f_1(s, d)^2} \tag{A6}$$

$$C_{gd} = \epsilon Z \frac{2L}{a} \frac{[-\frac{2}{3}(d^3 - s^3) + \frac{1}{2}(d^4 - s^4)](1 - d) - f_1(s, d)(d - d^2)}{f_1(s, d)^2}. \tag{A7}$$

In (A6) and (A7) and in the following unsymmetric transistors with one gate are assumed: L is the gate length and Z is the gate width. $f_1(s, d)$ is defined as

$$f_1(s, d) = d^2 - s^2 - \tfrac{2}{3}(d^3 - s^3). \tag{A8}$$

Equations (A6) and (A7) are plotted by long dashed lines in Fig. 3.

In the saturated velocity region we start from the total gate charge Q_g in [2, eq. (107b)]. By taking a partial derivative of Q_g with respect to V_{gd}, holding V_{gs} constant, one finds

$$C_{gd} = \epsilon Z(f_3 + f_4). \tag{A9}$$

Here, f_3 and f_4 are defined by

$$f_3 = -\frac{2W_{oo}}{f_1^2(s, p)} \left[f_1(s, p) f_2'(s, p) \frac{L_1}{a} + f_1(s, p) f_2(s, p) \frac{L_1'}{a} - f_1'(s, p) f_2(s, p) \frac{L_1}{a} \right] \tag{A10}$$

$$f_4 = -2W_{oo} \left[-\left(\frac{p}{a} + \frac{\xi}{2L} \sinh\left(\frac{\pi L_2}{2a} \right) \right) L_1' + \frac{L_2}{a} p' \right]. \tag{A11}$$

The primes in (A10) and (A11) indicate derivatives with respect to source-to-drain voltage. f_1 is defined as in (A8), except by replacing d with p. f_2 is given by

$$f_2(s, p) = \tfrac{2}{3}(p^3 - s^3) - \tfrac{1}{2}(p^4 - s^4). \tag{A12}$$

L_1 and L_2 are the lengths of the channel where the carrier velocity is unsaturated and saturated, respectively. Of course, $L_1 + L_2 = L$. Expressions for L_1 and L_2 as a function of s and p may be found in [2]. After some algebraic manipulation one finds

$$f_1'(s, p) = 2p(1 - p)p' \tag{A13}$$

$$f_2'(s, p) = pf_1'(s, p) \tag{A14}$$

$$p' = \frac{f_1 - \left(\frac{L_1}{L}\xi\right)^2 \frac{1}{f_r}\cosh\left(\frac{\pi L_2}{2a}\right)}{W_\infty 2p\left[(1-p)\frac{L_1}{L}\xi\cosh\left(\frac{\pi L_2}{2a}\right) - f_1\right]} \tag{A15}$$

$$\xi = \frac{E_s L}{W_\infty} \tag{A16}$$

$$f_r = \frac{1}{1-p}\left[\left(2p(1-p) + \xi\frac{L_1}{L}\right)\cosh\left(\frac{\pi L_2}{2a}\right) - 2p(1-p)\right] \tag{A17}$$

$$L_1' = \frac{2pL_1\left(1 - p - \xi\frac{L_1}{L}\frac{1}{f_r}\right)}{W_\infty 2p\left[(1-p)\frac{L_1}{L}\xi\cosh\left(\frac{\pi L_2}{2a}\right) - f_1\right]}. \tag{A18}$$

The quantity C_{gs} can be obtained from the total gate capacitance C_{gg} (derived in [2, eq. (109)]), according to

$$C_{gs} = C_{gg} - C_{gd}. \tag{A19}$$

In the present notation we find

$$C_{gg} = \epsilon Z\left[\frac{2}{f_1(s,p)}\frac{L_1}{a}\left(f_g\frac{2p^2(1-p)^2 + f_2}{1-p} - s(1-s)\right) + 2\frac{L_2}{a}f_g + (1 + 2pf_g)\left(2\frac{L}{a}\frac{1}{\xi}\frac{p}{\cosh\left(\frac{\pi L_2}{2a}\right)} + \tanh\left(\frac{\pi L_2}{2a}\right)\right)\right] \tag{A20}$$

where f_g is now defined as

$$f_g = \frac{(1-s)\cosh\left(\frac{\pi L_2}{2a}\right) - (1-p)}{\left[2p(1-p) + \xi\frac{L_1}{L}\right]\cosh\left(\frac{\pi L_2}{2a}\right) - 2p(1-p)}. \tag{A21}$$

In Fig. 3, C_{gs} and C_{gd} from (A9)-(A21) are shown as solid lines.

The formulas in (A9) and (A20) do not contain the fringing field corrections which become important for gate lengths of 1 μm and less. Following [2], C_{gg} in (A20) should be increased by adding $\epsilon Z(\pi/2)$, allowing for field fringing from the gate toward both the source and the drain. Similarly, the expression of (A9) should be augmented by $\epsilon Z(\pi/4)$ to correct for field fringing towards the drain.

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APPENDIX C

DESIGN PLANS

SOME CIRCUIT PARAMETERS REQUIRED FOR CAD MODELING AND ANALYSIS OF E3 IN MMICs

Microwave Integrated Circuit Parameters

The microwave circuit parameters which are used to model MMICs are user inputted data to CAD software programs like SUPERCOMPACT, TOUCHSTONE, MICROWAVE SPICE, and LIBRA. These parameters are attributes (or, characterizations) of both the active devices and the passive, transmission line structures used in MMIC models. They provide the numerical values of the circuit elements in the computer models that are used to "mimic" or simulate microwave function(s) and the associated circuitry in the MMIC of interest.

The term "device" is defined here as a packaged entity which performs a single microwave circuit function such as a two stage, low noise pre-amplifier or a four stage, power amplifier. The packaged MMIC device will usually contain one or more active, semiconductor chips (usually, GaAs FETs) mounted and wired together on appropriate ceramic substrates.

In addition, there will also be the associated transmission lines on both chip(s) and substrates to provide the necessary coupling and tuning elements for realizing the particular microwave circuit function. Finally, there are the biasing and ground rails with capacitive and inductive, RF bypass filters.

The device parameters are normally measured but in some cases may also be computed from the device physics. This involves formulating and solving some very basic and complex linear and nonlinear, partial differential wave equations and diffusion equations with more often than not, time varying boundary conditions.

This sort of theoretical approach to device modeling is best left to the device physicists. We recommend an empirical approach to measure the necessary circuit parameters required for CAD modeling and analysis software as user input data.

Measurement Ports

The parameters seem to fall into two categories; those measured externally at the ports of the packaged MMIC and those measured internally at IC and other nodal ports. These latter involve delidding the MMIC package, depassivating the chip(s), etc., in an inert environment to make probe measurements of the GaAs FET's and the passive microwave circuitry contained on/in the chip. We call these two categories of port measurements as external port and internal node measurements, respectively; or simply "external and "internal" ports for short.

The following lists of parameters were compiled from LIBRA and TOUCHSTONE documentation. In addition, available circuit files on the LNA's and PA's for both Rome Laboratory T/R module work and the MMIC DARPA/DoD initiative work which provided by Raytheon were also used. Some of these files contained netlist and layout data parameters for circuit designs and use SUPERCOMPACT, offering a possible perspective on a CAD program different than either LIBRA and TOUCHSTONE.

In addition, the parameters identified are for both the baseline and E3 modeling requirements. The "baseline" refers to those data required to model the MMIC's design-to-performance, the so-called intended functional design. The "E3" modeling requirements refer to those data parameters that are used to characterize the deviations from the baselines. These latter are usually the interference effects.

For example, the third order power intercept is measured in -dBm's of input power as a function of the output power. It is a common characteristic of an amplifier going into 1 dB of saturation (in its output power) because of nonlinear mixing effects in the amplifier which is caused by the E3 power at the input port. This 1 dB level below saturation is considered a practical (upper) limit on the dynamic range and anything less is treated as a deviation from the desired baseline performance.

I. BASELINE MEASUREMENTS: EXTERNAL PORTS

PARAMETER	SYMBOL	COMMENTS
Complex input reflection coefficient	S11	small signal, bias independent
Complex forward transfer coefficient	S21	small signal, bias independent
Complex reverse transfer coefficient	S12	small signal, bias independent
Complex output reflection coefficient	S22	small signal, bias independent
Large signal S parameters	S11, S21 S12, S22	power dependent bias dependent
Noise Figure and other noise related parameters	N.F.	bias dependent
Dynamic Range	DR	bias dependent
DC/RF Efficiency	eta D.C.	RF pwr/DC pwr in bias dependent
Power Added Efficiency	eta A	(RFin-RFout)/DC pwrs; power and bias dependent
Pkg Resonance Factors	Q1, Q2, Q3, etc.	inband and out-of-band bias dependent
Pkg Q Frequencies	Fr1, Fr2, etc.	bias dependent
Fixture and connector embedding parameters	S parameters, as appropriate	bias dependent, large and small signal dependent

II. BASELINE MEASUREMENTS: INTERNAL NODES

BJT PARAMETER	SYMBOL	COMMENTS
Current gain, Beta	B	Magnitude @ D.C.
Current gain, Alpha	A	Magnitude @ D.C.
Phase Angles	phi sub B phi sub A	Beta Alpha
Time Delays	Tau sub B Tau sub A	Beta delay ps Alpha delay ps
Bandwidth, alpha control	Delta F sub A	3 dB frequencies
Bandwidth, beta control	Delta F sub B	"....."
Collector capacitance	CC	Picofarads
Collector conductance	GC	Siemens (or mho)
Base resistance	RB	Ohms
Base inductance	LB	Nanohenries
Emitter capacitance	CE	Picofarads
Emitter resistance	RE	Ohms
Emitter inductance	LE	Nanohenries
Emitter lead inductance	REL	Nanohenries

FET PARAMETER	SYMBOL	COMMENTS
Transconductance	G	Siemens (or mho)
Time delay	T	transconductance
Roll-off frequency	F	GHz, MHz, kHz, etc.
Roll-off Slope	Delta G/delta F	dB/octave
Gate/Source capacitance	CGS	Picofarads
Gate/Source conductance	GGS	Siemens (or mho)
Channel resistance	RI	Ohms
Drain/Gate capacitance	CDG	Picofarads

Drain/Source capacitance	CDS	Picofarads
Drain/Source resistance	RDS	Ohms
Dipole layer capacitance	CDC	Picofarads
Source resistance	RS	Ohms
Gate resistance	RG	Ohms
Noise parameters	P,R,C,Kr,Kg,Kc K1,K2,K3,K4,K5	LIBRA referenced
Drain/Source voltage	Vds	chip bias, volts
Gate/Source voltage	Vgs	chip bias, volts

III E3 MEASUREMENTS: EXTERNAL PORTS

PARAMETERS	SYMBOL	COMMENTS
Harmonic Distortion	User Option	all signal ports all in/out pairs
Intermodulation Distortion	User Option	"
Crossmodulation Distortion	User Option	"
Desensitization	User Option	"
Gain Compression	User Option	"
Gain Expansion	User Option	"
Nth Order Intercepts	P13,P15, etc.	for N=3, 5, etc. bias dependent
E3 Vector Distortion*	User Option	at all the port pairs in all the combinations of any accessible ports including bias, grnd, and digital ports.

* "E3 Vector distortion" in an operating multi-port device is defined as the response at any port in which a deviation from its baseline performance is caused by E3 as a source vector connected to any other port. "Baseline performance" of a device is defined as its measured normal operating parameters or the "designed-to" specifications of the device. "Admissible ports" are all the accessible ports or pin pairs on the device package when operating as intended.

Even and odd mode impedances	Z sub e Z sub o	coupled lines
Even and odd mode dielectric constants	K sub e K sub o	coupled lines
Even and odd mode attenuations	A sub e A sub o	coupled lines
Coupler length	L	coupled lines
Lossy capacitor	CAPQ	discrete element
Quality factors	Q sub C Q sub L	discrete C discrete L
Lossy inductor	INDQ	discrete element
Bias voltage supply	Vdd	pkg port (pins)
Bias current drain	Idd	pkg port (pins)

DEFINING AN ELECTROMAGNETIC ENVIRONMENT FOR PREDICTING T/R MODULE SUSCEPTIBILITY: A DATA ACQUISITION PLAN

1. Purpose:

The purpose of this plan is to identify data needed to define the environment of ambient electromagnetic fields and spectra that are incident upon an aircraft radar surveillance platform with a phased array antenna which uses T/R modules in its active aperture.

2. Definitions:

"electromagnetic environment" - spectral, spatial and temporal distributions of electromagnetic energy or power in which a given system, equipment, device, circuit or component must operate while performing its specified, "designed-for" function.

"spectral, spatial and temporal distributions" - empirical data or the analytical algorithms for generating such data that provide electromagnetic energy profiles in terms of field attributes at given coordinates and locations above the earth, and at specified times or durations: these include intensities, phases, polarizations, average and/or peak power levels, spectral and/or spatial power densities, RF carrier and harmonic frequencies, etc.

"platform" - a description of an emitting and/or receiving structure, vehicle or configuration that includes the geometrical, electrical, physical, avionics and other databases needed to analytically identify and characterize the entry ports of electromagnetic energy.

"electromagnetic environmental effects (E3)" - spectral and temporal responses of a system, equipment, device, circuit or component that are caused by the electromagnetic environment and that degrade, compromise, prevent or otherwise alter the victim's "design-to" performance in its intended environment: the effects may be temporary or permanent.

"E3 drivers" - Thevenin and Norton circuit models that characterize the electromagnetic environmental fields and spectra on the victim platform as equivalent, dependent voltage and current sources that provide ambient environmental energy and power signals to the susceptible ports of entry.

"category I effects" - responses that could result in the loss of life, loss of the platform, a "costly" abort (in the Gigabucks range) or an unacceptable reduction (or loss) of functional performance that <u>will</u> jeopardize the system effectiveness.

"category II effects" - responses that could result in injury, damage to the platform or a reduced functional performance that may jeopardize the system effectiveness.

"category III effects" - responses that could result in annoyance, discomfort or a reduced functional performance that may not jeopardize the system performance.

"category IV effects" - responses that could enable the compromise of classified and/or proprietary data, or the characteristics of the systems and equipment that transmit, receive, store, process, display, print or otherwise handle such data.

"category V effects" - responses that could enable the unauthorized access, manipulation or theft of financial assets, or the characteristics of the systems and equipment that transmit, receive, store, process, display, print or otherwise handle such assets.

3. Data Sources: Candidate sources for a first cut at these data are suggested as:

1) ECAC in Annapolis, MD
2) ROME LAB/IRAE (W. Hartnett)
3) ROME LAB/EE (thru ERPT's on-going programs)

4. Data Restrictions: Unclassified data are preferred.

5. Data Formats: Data should be format compatible with Rome Lab GEMACS fields type analysis tools.

6. Frequency Range: 100 MHz to 50 GHz.

7. Bandwidth Range: Spectral bandwidths of the power, energy or fields' distributions as available in % bandwidth or as a centered frequency range.

8. Altitude Range: 20 kFt to 60 kFt.

9. Type Fields: whatever fields data are available: i.e., electric, magnetic or both.

10. Intensity Levels: whatever field intensities are available: i.e., dBuv/m.

11. Power Levels: whatever power levels are available: i.e., dBm or dBm/cm^2.

12. Polarization: horizontal, vertical, circular, elliptic, random or otherwise.

13. Modulation: modulation characteristics, if available (i.e., CW, AM, FM, PCM, PN, PM, percent modulation, etc.)

14. Type Sources: types of sources generating the environment, if known (i.e., commercial radio and TV, military radar, amateur, etc.)

15. Precipitation Static Levels: average and peak lightning activity in the locale as field levels, if available.

16. Locations: Geographical locations suggested are; 1) Mideast, 2) Northern Europe, 3) Former USSR Republics, 4) Former Yugoslavia Republics, 5) Central Europe, 6) Southwest Asia, 7) Far East, 8) Central America, 9) Northeast Asia

17. Areas: Areas of interest within a global location are:

1) urban
2) rural

18. Temporal Variations: The time variations in the data are of interest, if available:

1) seasonal: i.e., four seasons, averaged over 3 months.
2) weekly: i.e., average of any seven consecutive days.
3) daily: averages of 24 hour periods.

19. Topographies: Natural topographies of interest, if available, are:

1) flat, treeless
2) flat, treed
3) hilly
4) mountainous
5) sandy
6) gullied
7) canyoned
8) marshy
9) deltas
10) salt water
11) fresh water

20. Other:

Any other descriptions of the natural environment and its electromagnetic sources that can in any way relate with the electromagnetic characterization of a vehicle or platform immersed in such an environment.

21. NOTES:

DESIGN AREAS IN T/R MODULES OF CONCERN DUE TO E3 IN MMICs

Background

T/R modules in phased arrays of advanced design, active aperture radars must be robust to operate and survive in wideband, spectrally dense (E3) signal environments. Intrusive coupling from high power, exterior sources, friendly and otherwise, cause upset, distortion and damage in the digital ICs and linear MMICs of a victim module.

Additionally, parasitic coupling of unintended internal sources that interact with a modules' nonlinear circuits, outside of its design bands, produce degrading mix products in-band. The sum result is a synergism of E3 effects and a decreased effectiveness of the array and its host radar. We list below some design areas of concern for T/R module and MMIC environmental interactions.

E3 Design Caveats

1. T/R module and MMIC packaging effects from parasitics and internal field resonances must be avoided.

2. Control stray mutual coupling impedances between radiator elements for stable patterns.

3. Seek internal trace and ground plane layouts for minimal coupling.

4. High speed digital clocks are sources of spurious emissions: avoid where possible.

5. High dynamic range increases IMOD and XMOD susceptibility.

6. Analog signal processing demands minimal distortion in the desired signals' spectra.

7. Common mode grounding among MMIC devices, hybrids, digital circuits and striplines must be avoided.

8. ESD protection networks for MMIC GaAsFETs are susceptible to E3 even when quiescent in the untriggered mode.

9. Short run lengths to minimize stray inductive coupling and radiation are a must.

10. RF bypass capacitors, vias and other interconnects must be linear.

11. Find component layout strategies for a minimal E3 topology.

12. High speed, high density clock lines are sources and sinks of radiation emission and susceptibility.

13. Digital offset, latchup and ground bounce all effect the antenna pattern integrity.

14. Signal harmonics and intermodulation products into any MMIC port can cause distortion and upset.

15. Trace and stripline geometries must be gradual to minimize any emission or coupling at sharp bends.

16. Imbedding ports for MMIC self-test adds circuits which may be more susceptible to the E3 than the baseline MMIC host.

Note: some of these concerns may overlap; some may be the domain of functional designers - they are included for completeness.

Historical Concerns

During a recent T/R module development program, it was reported that early prototype designs were deficient. Internal parasitic effects at microwave frequencies contributed to the Q of the resonant cavity formed within the module itself. The cavity was driven by RF leakage from the transmitter channel into the receiver causing unacceptable module performance. The design fix added ferrite absorbers into the transmitter cavity to despoil its high Q. The fix worked but added more components to the module with attendant cost penalties.

In designing phased array antennas, one attempts to locate elements close enough to each other in order to synthesize the static pattern without contending with the mutual coupling effects which tend to break up the pattern. The design rules for the radiator separation are usually based on the operating wavelengths. These criteria are "in-band".

However, the input impedances of modules can go nonlinear if subjected to high enough input power levels from any nearby transmitting elements in the environment, or from any other RF sources which may be also on the same platform. The latent nonlinearities in FET's, circulators and diode switchs can contribute unintended mix products, in-band and out-of-band, which cause unacceptable distortion in the desired signals.

A module designer likes to keep his circuit layouts very compact in order to reduce the volume and weight overhead, to reduce the thermal paths to the heat sinks and to minimize the stray, internal coupling. This consideration is usually in-band and the (design-to) trace separations are usually based on those wavelengths for the unwary designer. Unfortunately, this design strategy does not account for the circuit nonlinearities which can produce strong coupling at many unsuspected frequencies.

In addition, coupling caused by radiation from the traces onto the DC rails with only nanohenries of inductance, causes common mode noise to build up in the power conditioner, possibly degrading the noise margins in the digital controller circuits. Upsetting the phase shifter bits degrades the antenna pattern.

Emission levels from clocks and LO's can also couple onto the traces and transmission lines, and be conducted into susceptible FET's and logic IC's. Ground bounce is another problem in the digital circuits of these modules.

Ground bounce occurs when a voltage builds up on a trace inductance from fast current switching transients, causing the gate "low" state to seek one of two (or more) grounds i.e., the digital chip or the external ground plane. This ground hunting causes degraded BER, enhanced emissions, circuit ringing, and other circuit stresses.

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